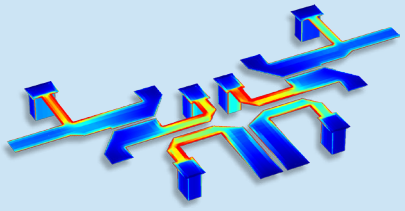
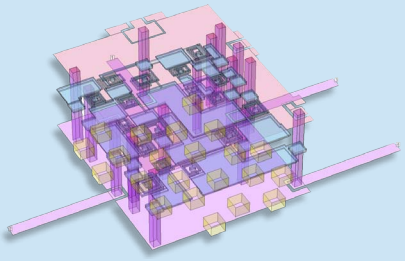
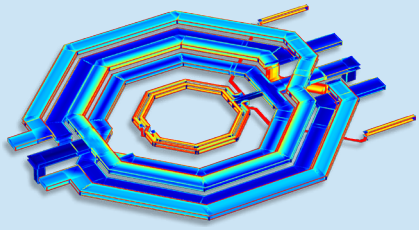
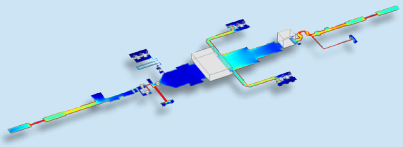
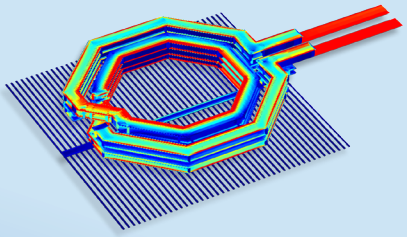
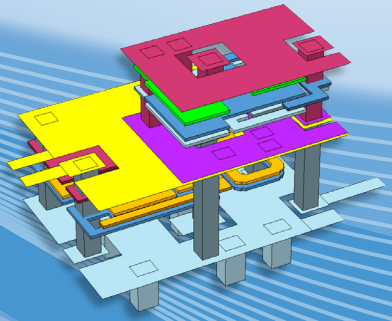










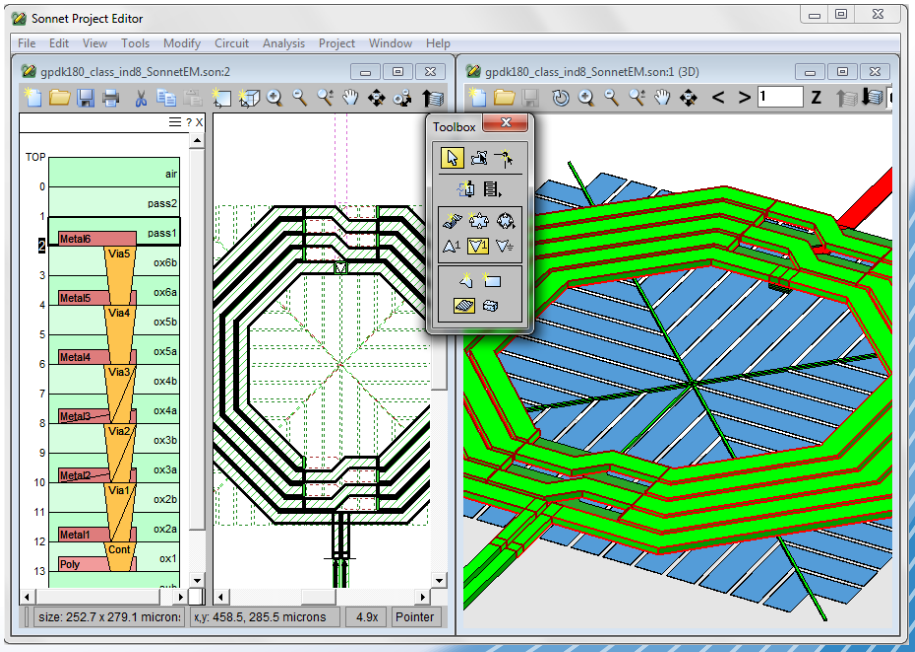


SONNET®

Going with the Flow

Sonnet Professional Suite Release 14

With Release 14, the Sonnet Professional Suite puts fabrication-accurate high frequency electromagnetic (EM) extraction models into your EDA design flow. New features and enhancements in this release provide faster simulation, ability to conquer larger circuits and layouts, and a more automated design flow through the EM extraction process.



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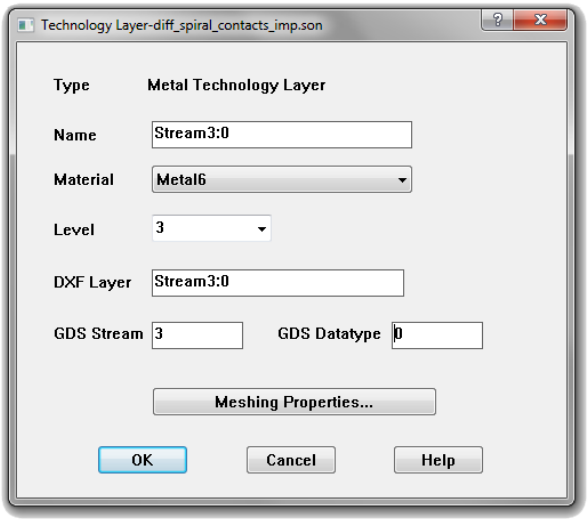
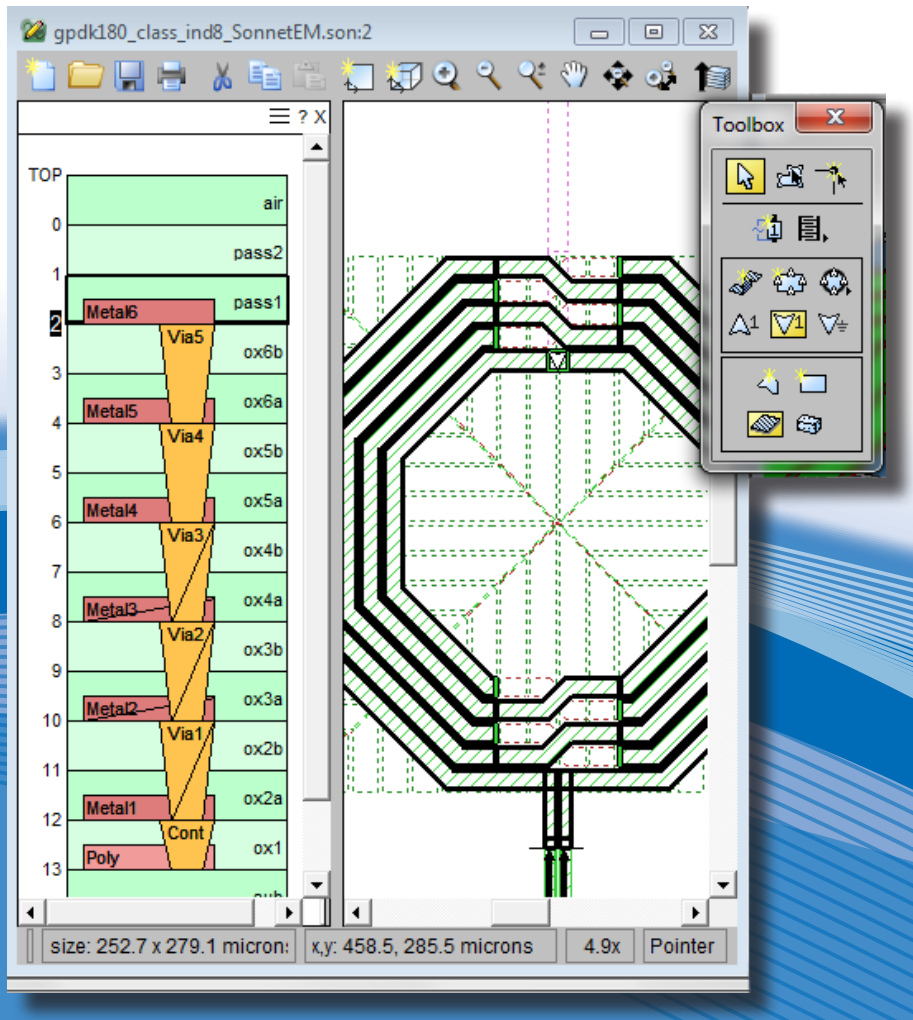
Technology Layers for Design Flow Integration



Technology Layers are introduced in Release 14 to enable smoother transition with EDA frameworks and design flows. A Technology Layer is a definition for associated objects in your Sonnet EM projects, which groups common attributes such as a layer name, physical location within the technology stackup, metal properties, and meshing controls. Technology Layers may be defined for planar metal, vias and dielectric bricks. They can also be defined automatically by GDSII or DXF Imports, on a one-to-one basis with GDSII stream or DXF layer names—thus giving Sonnet the ability to preserve CAD layers from your source tool in both import and export. Technology Layers make it possible for you to retain the same drawing layers that you may be using in your RF design framework, without need to redefine them in Sonnet.

Stackup Manager

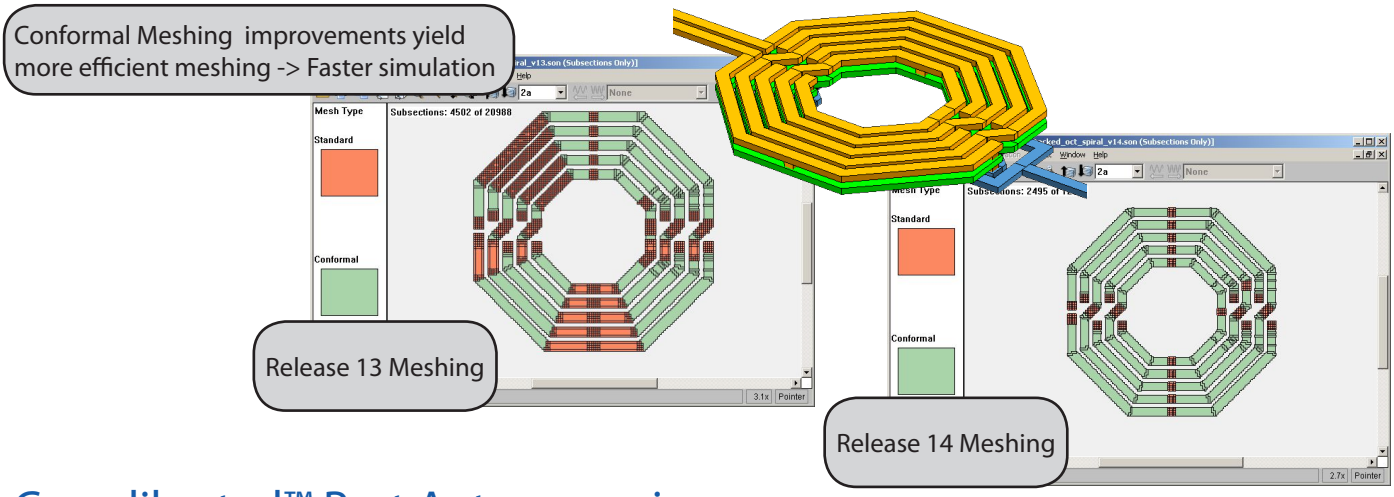
A new Stackup Manager panel has been added to the Sonnet Project Editor, providing an intuitive interface for creating or editing the process stackup. It also provides a graphical interface to manage the new Technology Layers in Sonnet. Using the Stackup Manager, an inexperienced user can quickly locate their process drawing layer in order to edit or modify circuitry at the correct location in the stack. The Stackup Manager is automatically populated when the Sonnet Project Editor is called by our interfaces to Cadence® Virtuoso® and Agilent ADS™.



Faster Simulations

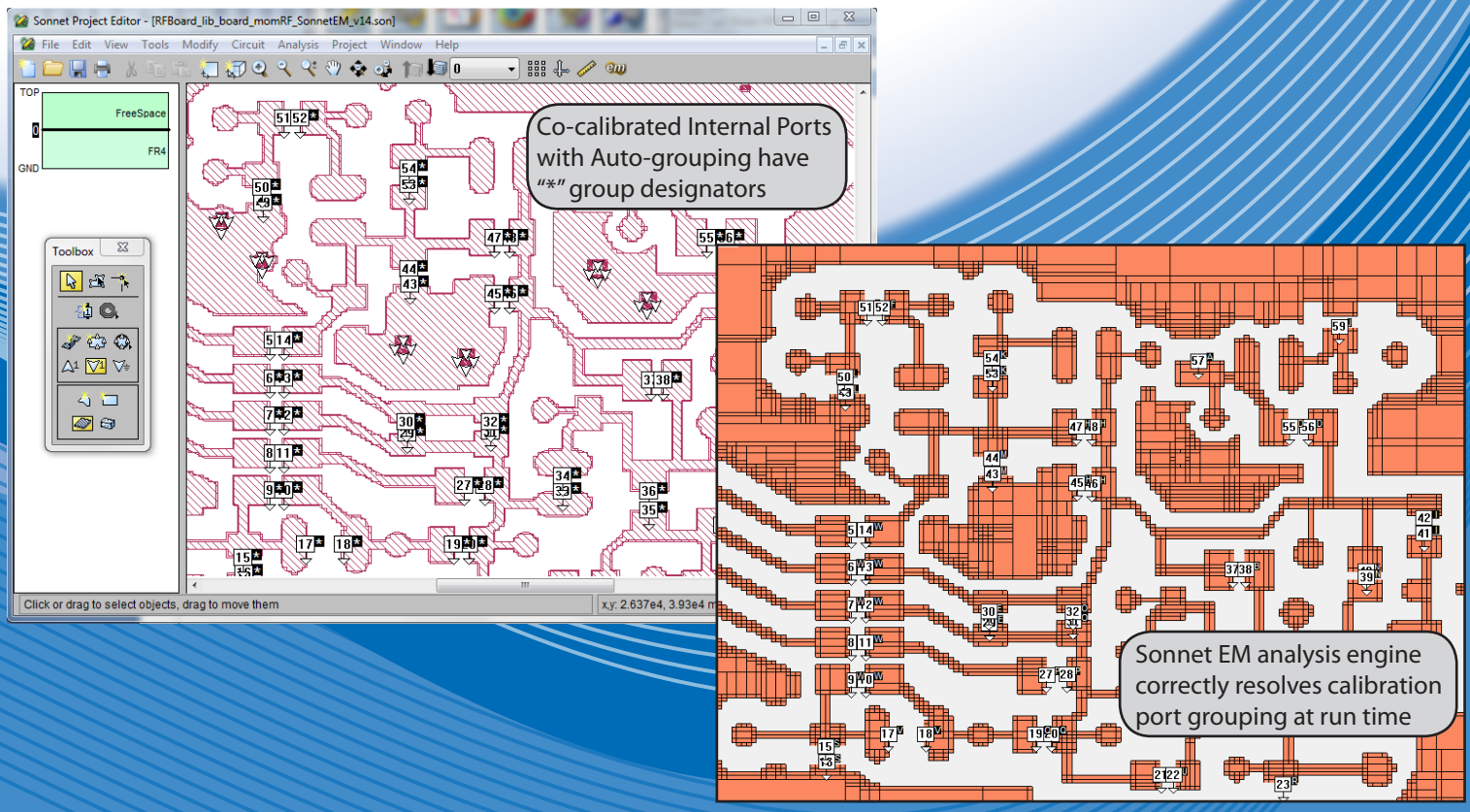
Sonnet is keeping pace with high performance CPU development, and our Release 14 EM solver engines are faster than ever before. In our Desktop Solver engine, we have increased the parallel CPU core utilization from 3 to 6 cores, resulting in nearly 2X faster simulations. Our High Performance Solver has been increased from 12 to 32 CPU cores in parallel, enabling high-end computing hardware to deliver ultra-efficient simulations.

In addition to increased CPU core parallelization, our meshing algorithms have also been tuned to yield high solver efficiency. Large-scale IC via arrays and via bar structures are more efficiently meshed for accelerated simulation of deep-node silicon RFIC circuits and interconnects. Our patented conformal meshing technology has also been enhanced for higher efficiency when simulating stacked and thick metal structures.



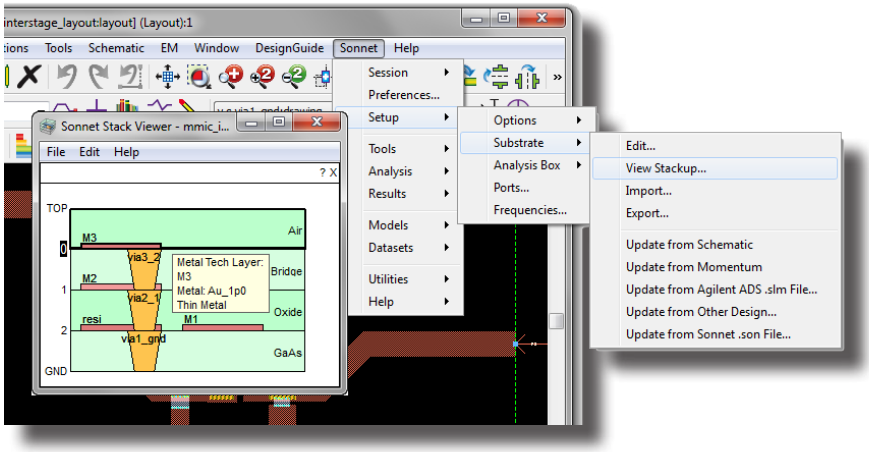
Co-calibrated™ Port Auto-grouping

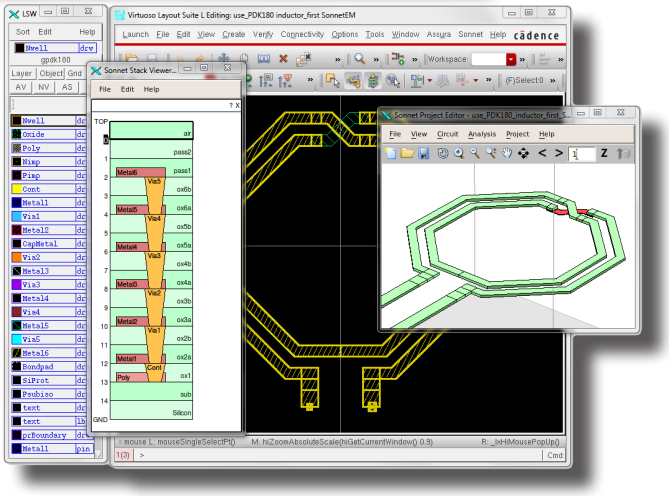
Sonnet's Co-calibrated Ports provide unprecedented accuracy for internal port calibration, enabling error-free access to internal connections for large circuits. To fully leverage this capability in past releases, the engineer would manually group closely-spaced ports into calibration groups. In Release 14, we introduce Co-calibrated Port Auto-grouping, a feature that relieves the designer of manual work by giving the solver intelligence to group ports automatically and accurately at run-time. Just set your Co-calibrated internal port group settings to "Auto" and let the solver worry about grouping.



EDA Framework Interface Enhancements

RF engineers using the Cadence Virtuoso or Agilent ADS platforms will notice increased automation for Sonnet's seamless integration products. With enhancements such as Co-calibrated Port Auto-grouping and Stackup Manager access from within the interfaces, Sonnet allows for truly streamlined 3D planar EM model extraction without breaking the flow. Sonnet's EDA Interfaces to Cadence Virtuoso and Agilent ADS now include:

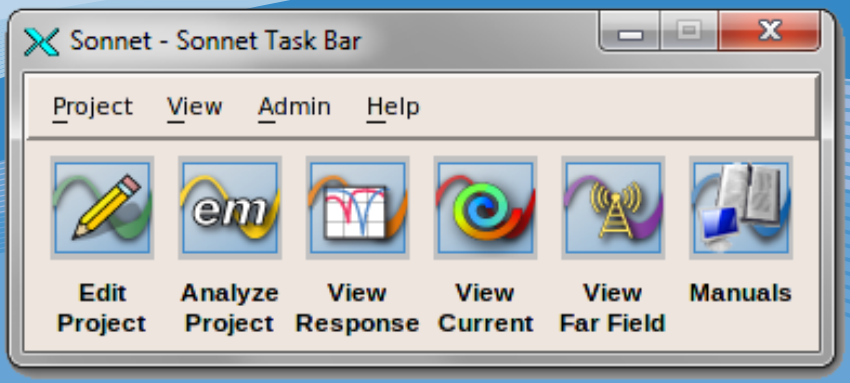




- Automatic population of Sonnet Technology Layers from Cadence and Agilent Drawing Layers
- A Stackup Viewer for intuitive technology stackup display inside the EDA framework
- Direct access to the Sonnet DC continuity checker from within the EDA framework
- Co-calibrated Port Auto-grouping is automatic for internal ports
- Save/Load States moved to Virtuoso Cell View
- Option for union of via polygons after via simplification and merges to further reduce meshing requirements of micro via arrays
- Via array merging added for substrate contact vias without bottom planar metal

Enhanced GUI performance for Linux and VM software hosting

Sonnet Release 14 provides GUI updates to meet the growing need for deployment on Linux and VM host hardware platforms. The Sonnet Suites Release 14 interfaces have been tuned for fast response over remote host and VM host networks—increasingly important for enterprise-level installations.



Sonnet Task bar on Linux OS

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