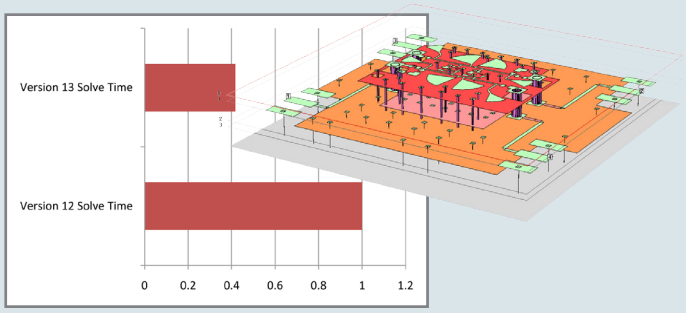
SONNET® New Features in 13

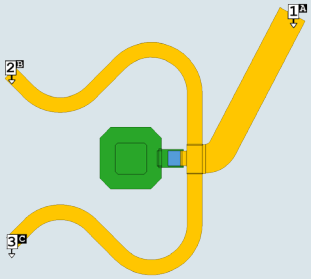
Faster Large Circuit EM Analysis

Sonnet is keeping pace with high performance multi-core CPU development, and our Release 13 solver engines are faster than ever before. Algorithm improvement and further parallelization for our 64-bit solver engines yield significant improvement in the analysis of large (> 3GB) simulations. In the hybrid package analysis shown below, our High Performance Solver is nearly 60% faster in the new release. Sonnet's budget-friendly Desktop Solver (DTS) engine has been increased from using 2 to 3 CPU cores in parallel, and our High Performance (HPS) engine has been increased from 8 to 12 parallel cores.



Sonnet's ***emCluster*** product can also be used to combine multiple computing platforms to cut EM simulation times further through parallel cluster computing. When EM simulations are mission critical, Sonnet's ***emCluster*** computing model with multiple HPS engines can reduce large simulations from hours to minutes.

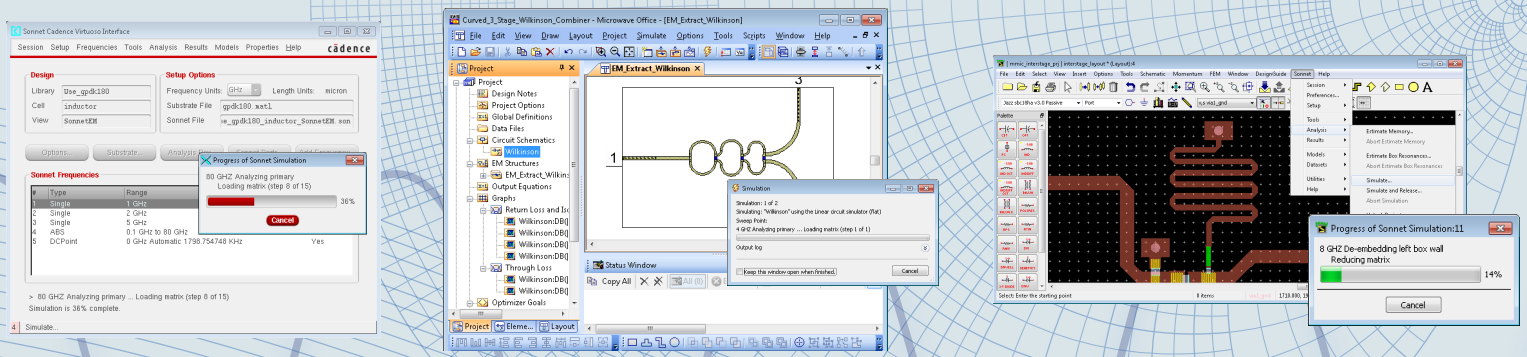
Diagonal Ports



Not all circuits have ports that are neatly aligned in vertical or horizontal directions. In Release 13, we introduce diagonal ports, so you can set both edge ports and internal ports tipped at any angle to fit your circuit geometry. Rotated SMD components for RF PCB and package analyses are also now possible. Diagonal ports give you unprecedented freedom for design partitioning, and allow for unique internal circuit connections at any direction.

Enhanced RF EDA Integration

One of Sonnet's strengths is interoperability with all major RF EDA design frameworks. Sonnet can be used both as a standalone 3D planar EM simulator, or as an EM engine client that is employed entirely within your RF EDA design framework. We provide seamless integration with Cadence Virtuoso, Agilent ADS, and AWR Microwave Office. In Release 13, our interfaces to the RF EDA frameworks have been enhanced and further automated, making it simple and easy to incorporate Sonnet in your RF layout design/analysis flow. The incorporation of "States" for our interfaces now make it possible for you to save Sonnet settings for a given process technology, so you can quickly recall them for future designs.



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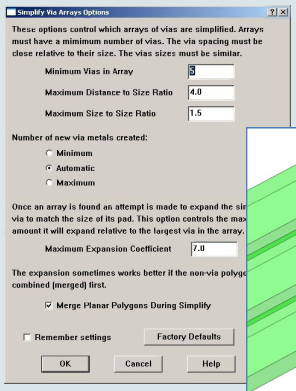
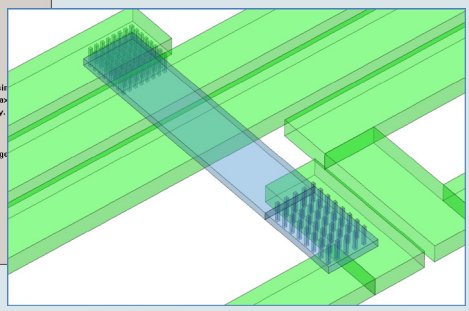
Simplified Via Arrays

Today's RFIC processes employ large arrays of vias for creating layer-to-layer interconnects, and for developing multi-layer transmission line metal "stacks" to reduce losses. These via arrays, often composed of thousands of tiny vias, create special challenges for full wave EM solver meshing. Meshing each individual via for simulation leads to very high memory requirements due to the many small physical features.

In this new release, micro via array simplification technology is introduced to accurately model via array interconnects in a highly efficient composite manner. The simplification comes in the form of a new via fill type defined for the EM solver. The simplification is automated and accessible in our GDSII import, as well as in our RF EDA framework interfaces. Multi-layer planar metal stacks (such as those used in silicon RFIC inductors, baluns and transformers) can now be efficiently simulated in Sonnet without manual model adjustments.





Increased Memory & Features for entry-level Suites

Sonnet Lite, LitePlus, and the Level2 Suites can now solve 40% larger problems* over the previous releases. These suites have a limitation imposed on the maximum amount of memory that is allowed to solve a given problem, and these limits have been doubled in Release 13, enabling the solution of even larger structures.

Sonnet Level3 Gold has been increased from 256 MB to 2000 MB, enabling you to solve 300% larger circuits*. More ports (including Co-calibrated ports), components and variables have also been added to these suites, adding value and more capability at a budget.

Sonnet Suites Comparison- Allowed Memory

	Release 12	Release 13
Lite *	16 MB	32 MB
LitePlus	32 MB	64 MB
Level 2 Basic	64 MB	128 MB
Level 2 Silver	128 MB	256 MB
Level 3 Gold	256 MB	2000 MB

* Registered copies only

* Circuit size measured in terms of mesh cell count

And Much More

- New Short-Open Calibration (SOC) technique for port de-embedding extends Sonnet's port calibration algorithms to even wider dynamic ranges
- Connectivity Checker implemented for easy visual check of electrical continuity of analysis mesh
- Conductor surface roughness loss modeling for microwave substrates
- Independent reference planes are now possible for multiple box wall and Co-calibrated internal ports
- Physics-based via model which is accurate from DC to high THz
- SonnetLab toolbox for integrating Sonnet 3D planar EM simulations in MATLAB
- Heat flux visualization for the Current Density Viewer
- New and enhanced Example Circuit Browser
- Automatically submit and disconnect all unfinished simulation projects in a Remote EM processing batch
- Automatic data recovery of finished Remote EM Processing batches

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