Simulating Bondpads Using the Sonnet EM Simulator

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Abstract: In this paper, the EM simulation of bondpads in planar semiconductor technologies is discussed. Simulation methods, different forms, sizes, metal depths and shielding options are analyzed and compared with respect to the parasitic capacitance. A modified shielding is proposed which reduces the parasitic capacitance by 20 %. Possible applications include more exact prediction of bondpad influences on RF circuits and reduced capacitance bondpads for broad-band circuits.

Keywords: EM simulation, bondpads, interconnect modeling

1. Introduction

With the continuous advances in scaling of planar integrated circuit (IC) technologies, operating frequencies and data transmission speed of ICs have steadily increased. In contrast, off-chip connection elements such as bondwires cannot be scaled down as far as on-chip elements for mechanical reasons. However, off-chip elements can be compensated on-chip by design if their properties are sufficiently well known in early stages of the design process. Thus, the importance of exact connection modeling increases.

One key on-chip element of connection modeling are bondpads. Their minimal size being determined by mechanical restrictions of the bonding process, the cause two major problems in radio frequency (RF) circuits; parasitic signal coupling to the input of the circuit through the substrate and parasitic capacitive load of the circuit output. While the former can be can be efficiently avoided using a metal plane on the lowest possible layer, this enhances the said parasitic capacitance. In traditional RF circuit design, this capacitance is comparably small and can easily be included in the output matching network without further impeding circuit performance.

In high-speed broadband designs and V-Band applications however, the bondpad capacitance becomes high enough to significantly impact circuit performance parameters such as bandwidth or output matching. It is therefore necessary to exactly predict and, if possible, to reduce the capacitance as far as possible.

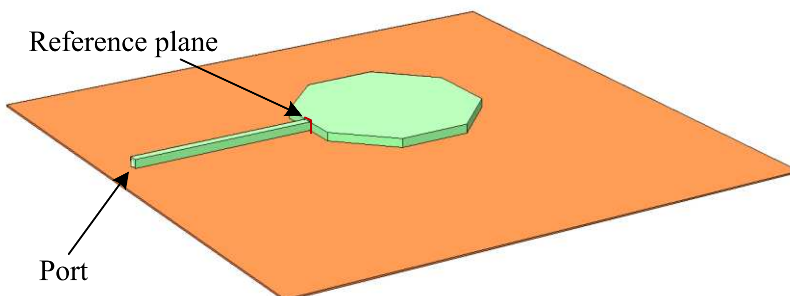


Fig. 1. Reference structure with port definition and reference plane.

2. Simulation Setup

A. Geometry

The simulation of bondpads in planar IC processes is demonstrated using the example of the 0.25µm BiCMOS IHP SG25H1 technology [1]. The technology offers two thick top metals for RF interconnects of which the topmost is used for bondpads. All EM simulations are done using the 2½-D simulator Sonnet [2]. Metals and dielectric layers were defined according to the IHP process specification using typical values [1]. Metals are simulated in multiple sheets to provide a higher accuracy. The reference structure is an octagonal bondpad of 60 µm diameter (see Fig. 1). This is the smallest structure that can be reliably bonded with state-of-the-art bonding processes.

B. Excitation and Deembedding

Excitation and deembedding of an isolated bondpad structure is difficult to be modeled in EM simulators. In nearly all practical cases, the bondpad is connected to the rest of the integrated circuit by a metal transmission line on the same metal layer and connected to the bondwire on nearly the entire top surface. It is therefore reasonable to consider the bondpad as one node with a parasitic capacitance to the ground plane but perfect transmission. For the EM simulation, the question arises where to introduce the excitation.

The most suitable option is to define the port at the box wall and to connect it with one single transmission line to the pad. The phase shift of the signal on the line can be removed by a shift of the reference plane to the bondpad edge and the capacitance of the line to the box wall can be deembedded by the Sonnet port calibration. As box wall port calibration is a mathematically simple step well implemented in Sonnet, this method of calibration is the most exact one. Although the marginal influence of the connecting line on the field under the bondpad is not removed by such a calibration, this field asymmetry will be equally existent in reality, so that the errors associated to the connection line are negligible.

C. Capacitance calculation

The S-Parameters are simulated from 0.1 to 100 GHz, Y-Parameters are calculated out of the S-Parameters. The capacitance is then calculated using [2]

$$C(f) = \frac{-1}{2\pi f \cdot \mathrm{imag}\left(\frac{1}{\underline{Y}_{11}}\right)}. \tag{1}$$

This formula assumes that the S-Parameter block represents a capacitance to ground in parallel to an ohmic resistor. As can be seen in Fig. 4, the value is constant at frequencies up to several ten GHz, justifying the assumptions made. The capacitance rises slightly towards higher frequencies because the bondpad then acts as a transmission line with open load. Although fundamental assumptions of the transmission line theory such as the transverse modes of the electromagnetic field do not hold for a bondpad, the model can be used to explain the frequency dependence of the capacitance. Simplifying the expression for the input impedance of a lossless transmission line, terminated with a load impedance $\underline{Z}_\mathrm{L}$ at a length l [3]

$$Z_{in}(l) = Z_0 \frac{\underline{Z}_\mathrm{L} + j \cdot Z_0 \tan(\beta l)}{Z_0 + j \cdot \underline{Z}_\mathrm{L} \tan(\beta l)} \tag{2}$$

for $\underline{Z}_\mathrm{L} \to \infty$ with the 3rd grade Taylor approximation for $\tan(\beta l), l \ll \beta$ and equating it with a the impedance of a series capacitance, one obtains the capacitance value

$$C(\omega) = \frac{l}{Z_0 \cdot v_\mathrm{ph}} \cdot \left(1 + \frac{l^2}{2 \cdot {v_\mathrm{ph}}^2} \cdot \omega^2\right), \tag{3}$$

where v_ph denotes the phase velocity on the line. As the bondpad is small compared to the wavelength for all practical frequencies, the term in ω^2 is negligible and independent of bondpad geometry, the materials or the simulating options, yet it explains that the capacitance is rising with frequency as shown in Fig. 4.

D. Discretization and Meshing

As with all simulators based on discretization of a given geometry, the choice of mesh greatly influences simulation time and results. In general, a finer meshing generates more exact results, however at the price of higher simulation time. In the specific case, where the shielding extends over the whole box, a high number of cells is created on the shielding plane making simulation time and memory very high, although it has only minor influence on the actual target value, i.e. the bondpad capacitance, because current densities on the shielding plane are low. A good starting value for a simple structure usually is a discretization of 256 by 256 cells yielding some 2000 subsections, 44 MByte of simulation memory and simulation times of some 20 min on a one-processor system.

Fig. 2. Meshing of the bondpad.

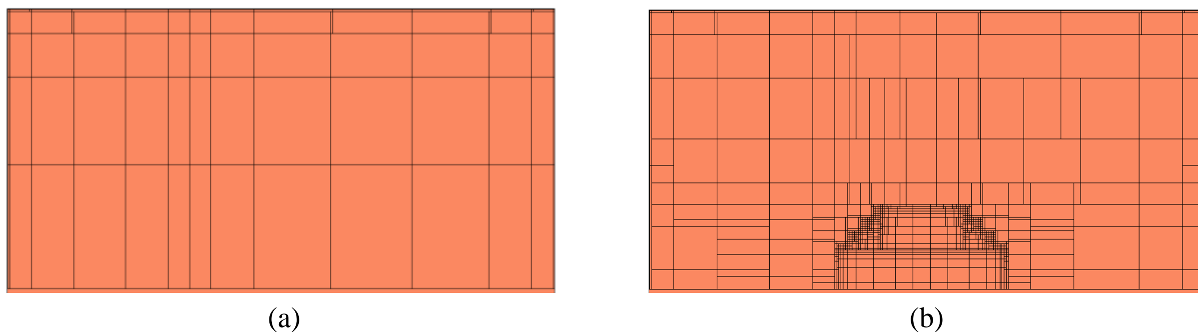
A second problem of the structure is inhomogeneous meshing. The bondpad is always edge-meshed, while the ground plane is – without any counter-measures – by default meshed uniformly (see Fig. 2). This causes high discretization errors as at the edges of the bondpad, a high number of (edge-meshed) cells is face-to-face with a single big cell on the ground plane, yielding incorrect simulation results. The solution to this problem is either a general decrease of cell size or an edge-meshing with automatic polygon edge checking on adjacent metallization levels, which are impractical due to simulation time aspects, or the insertion of a "ghost" structure directly underneath the bondpad. This is a copy of the bondpad polygon on the shielding plane forcing the mesher to edge-mesh the shielding plane accordingly (see Fig. 3(b) and (c)).

The most efficient solution is the definition of a dielectric layer with the thickness and properties of the metal plane. The solver then handles it as part of the boundary conditions of the problem, without creating more cells, therefore significantly reducing simulation time. Simulation results of the same reference structure with different meshing options are compared in Fig. 4 and Table 1.

TABLE 1: DIFFERENT MESH SETUPS

Setup	Cells	Shield	Simulation time (min)	Memory used (MB)
1	256×256	Plane	20	45
2	512×512	Plane	100	200
3	1024×1024	Plane	900	800
4	128×128	Ghost	8	43
5	128×128	Layer	1	7

Setups 1 to 3 show that the result is converging to a fixed and smooth capacitance curve with increasing number of cells, confirming the validity of the simulation. The insertion of the ghost delivers results very close to the reference result, but with much lower simulation time and memory.



(a) (b)

Fig. 3. Meshing of the groundplane with (a) default meshing options and (b) with ghost structure inserted.

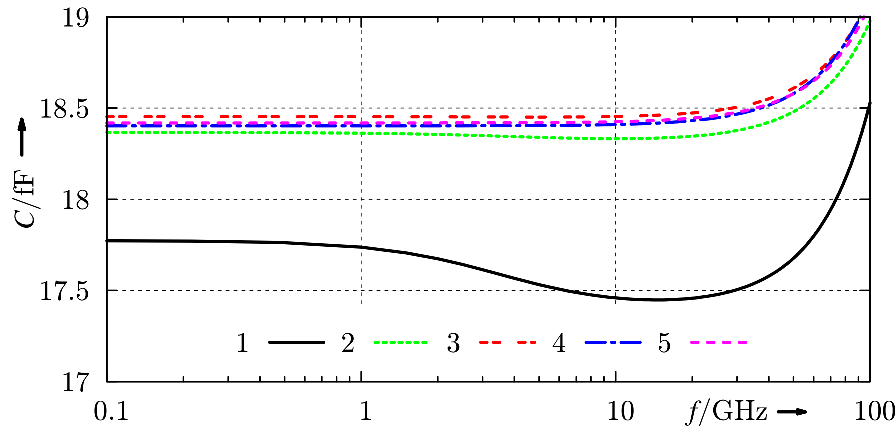


Fig. 4. Capacitance of bondpad model calculated using the different simulation setups from Table 1.

3. Varying Bondpad Geometries

A. Bondpad Size

Bondpad size was varied from 50 µm to 80 µm. The results are shown in Table 2. One can clearly see that the capacitance generally scales with pad area. Errors made estimating the capacity for pads of different sizes using the reference value would be below 10 %.

B. Bondpad Geometry

Two different bondpad geometries were simulated: rectangular and octagonal shapes. The results are also shown in Table 2. It is visible that the capacitance does not scale with size very well. The contribution to the inhomogeneous field outside the bondpad to the bondpad capacitance is obviously high. Therefore, different bondpad shapes will have to be modeled separately.

C. Anchoring Ring

In order to make the bondpad more robust against mechanical stress, for example occurring during the bonding procedure, bondpads are commonly "anchored" in the chip with a ring of metal on a deeper chip level and the corresponding set of vias. This obviously reduces the distance to the shielding plane on a significant part of the bondpad surface and therefore increases bondpad capacitance as can be seen in Table 2. The simulation results are compared using the equivalent area value, i.e. the area of a bondpad that is only on the uppermost metal layer, but has the same capacitance as the bondpad with the anchor ring assuming the electric field only has a component perpendicular to the bondpad. As one can see, this approach does not hold as the stray field at the edges of the bondpad and the edges of the anchoring ring significantly contributes to the capacitance. Therefore, to get correct values for the bondpad capacitance, the anchoring has to be considered.

D. Neighboring Pads and Seal Ring

Another question is whether the neighboring pads and the adjacent sealring are influencing the field distribution around the pads in a way to change the capacitance. As the main part of the field is doubtlessly between pad and shielding, one expects not to find any difference. A model was created including both neighboring ground pads and the sealring as depicted in Fig. 5(a). The groundpads are rectangular 80 µm pads positioned at a 100 µm pitch and the sealrings distance to the bondpad edge is 20 µm. Note that no further port needs to be introduced as all these structures are grounded by touching the box wall. The simulated capacitance of this structure is very close to the capacitance of the reference structure , so that the influence of neighboring pads and structures can reasonably be neglected in most practical cases.

TABLE 2: CAPACITANCES AT 0.1 GHZ FOR DIFFERENT BONDPAD GEOMETRIES

Size (µm)	50	**60**	70	80	60	60
Geometry	Octagonal				rectangular	octagonal
Anchoring Ring	None				none	TopMetal1
(equivalent) Area (µm²)	2286	**3291**	4480	5851	3600	4041
Capacitance (fF)	13.5	**18.4**	23.9	30.0	22.0	27.2
Capacitance/area (aF/µm²)	5.90	**5.59**	5.34	5.13	6.11	6.73

4. Different Shielding options

Shielding of bondpads from the substrate is very important for various reasons and different methods of realizing the shielding have been proposed [5], [6]. It is obvious, that a shielding plane should above all have a high conductivity and be as deep as possible in the chip. In addition to the solutions proposed in the literature, two options are thinkable satisfying the constraints:

1) A salicided substrate with p+ source/drain implant (PSD),
2) A n-well with a n-buried layer as used in bipolar sub collector and isolated NMOS devices

The first has a very low sheet resistance of only 5Ω, while the second is another 500nm deeper into the chip below the shallow trench isolation. However it has a very high sheet resistance, so that its shielding capabilities are questionable. Therefore, the first option is preferable.

A. Modeling of the Salicided Substrate with P+ Source/Drain Implant

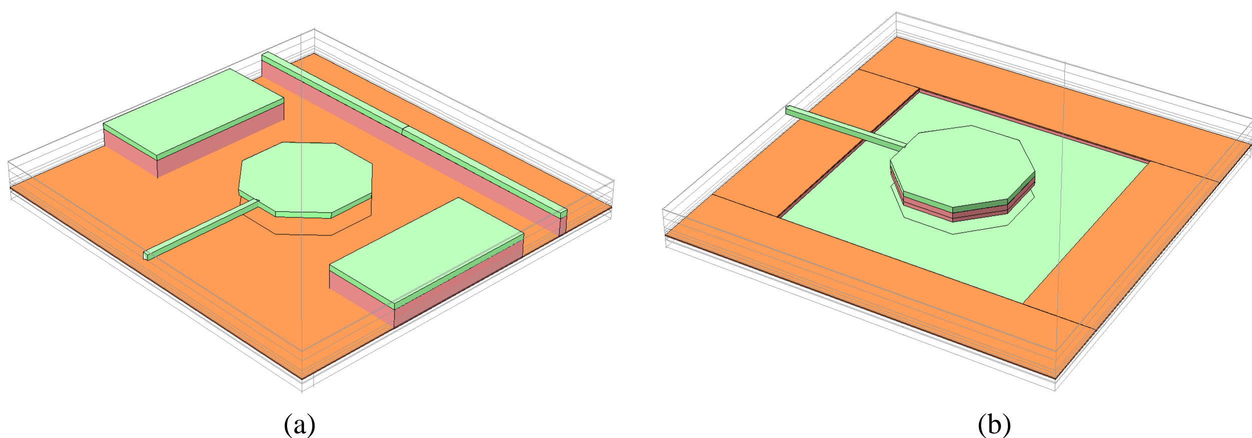
Sonnet offers the possibility of defining layers with given sheet resistances. The PSD layer perfectly fits in this category. However; the Process Specification Manual of the SG25H1 Process does not give information about the exact depth of a PSD implant, but being at least half as thin as a typical transistor stack, its thickness can be estimated to be below 100 nm. The second question is whether the skin effect will have any influence on the sheet resistance. The conductivity of the material is calculated using the assumed thickness

$$\rho = R_{\square} \cdot h \,, \tag{4}$$

and the skin depth is estimated using a standard approximation [4]

$$\delta(f) = \frac{1}{\sqrt{\pi\mu\sigma}} \cdot \frac{1}{\sqrt{f}} \approx 1.5\ \mu\text{m} \ @\ 60\ \text{GHz} \,. \tag{5}$$

It can be deduced that the current always penetrates the whole p+ source/drain implant. The sheet resistance approximation is therefore valid.



(a) (b)

Fig. 5. (a) Bondpad model including neighboring structures, (b) Realistic bondpad model.

B. Comparison to Common Shielding Plane

First, the shielding plane was assumed to cover the whole box as shown in Fig. 1. Simulation results show that the modified shielding reduces the capacitance from 18.4 to 15.8 fF, i.e. by approximately 15%. The estimation using the standard formula for homogeneous fields and the distances from the process specification was 20%.

5. Simulation of a complete realistic bondpad

Summing all influences investigated above is not possible. Therefore, a complete model of a realistic octagonal bondpad of 60 µm diameter including anchoring ring and p+ source/drain implant shielding plane with contacts (see Fig. 5(b)) and with a common Metal1-groundplane was simulated. The results are shown in Table 3. Compared to a realistic model using a Metal1-groundplane, the capacitance is reduced by 20 %. This value is higher than the value in the previous section, as for the area of the now included anchoring ring, the higher distance to the shielding plane becomes more relevant.

TABLE 3: CAPACITANCES FOR TWO REALISTIC BONDPDADS

Bondpad	60 µm Metal1	60 µm PSD-Activ
Capacitance at LF (fF)	27.1	21.7
Capacitance at 40 GHz (fF)	27.2	22.0
Capacitance at 60 GHz (fF)	27.5	22.2

6. Conclusion

This paper studies different bondpad structures using the 3D planar simulator Sonnet. Influences of different geometry aspects like bondpad size, bondpad shape and anchoring on the capacitance were studied. While coarse approximations of the influences with the standard capacitance formula for homogeneous fields are possible using corresponding bondpad areas, none of those aspects can be calculated with sufficient accuracy for broadband RF or V-band applications.

A modified shielding option was proposed which reduces the capacitance by approximately 20 % compared to the standard shielding using the lowest metal layer. A complex model of a realistic bondpad structure with the proposed shielding was created and simulated. The capacitance of such an octagonal 60 µm bondpad is 22 fF.

Acknowledgment

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