Sonnet EM Simulation of High Power Transformers for RF Power Amplifiers

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Abstract: Guidelines and challenges in designing on-chip transformers for radio frequency (RF) front-ends, especially for Power Amplifiers (PAs), are discussed. Multiple symmetric center-tapped high power transformers are designed in Cadence Virtuoso Layout XL using 0.13µm CMOS technology and EM simulated using Sonnet 13.54. Simulation results of the final design are also verified using the transformer equivalent model in Cadence SpectreRF. Results show good correlation between theoretical calculations and simulation data from Sonnet. Also, comparison between our various designs of transformers is made on the basis of number of turns, coupling co-efficient, self-inductances, winding resistance, quality factor and area. Our final design is used in a PA circuit that gives maximum 29dBm output power at 1.8 GHz with an overall efficiency of 52%.

Keywords: Center-tapped, EM Simulation, Fully Integrated Front-end, Impedance Matching, Power Amplifier, Sonnet, Transformer.

1. Introduction

Transformers have been a vital component in RF circuits for many decades. There have been multiple prior efforts to integrate transformer and/or baluns on-chip [1]. Previous work on on-chip transformers is best summarized in [2]. Numerous transformer layouts including parallel winding, inter-wound winding, overlay winding and concentric spiral winding were discussed. Depending on the application and frequency of operation, transformer design requirements can be quite different. For some low noise amplifiers (LNAs) and voltage controlled oscillators (VCOs), the transformer is optimized for optimal voltage gain and magnetic coupling. For PAs, the transformer is optimized to provide high efficiency at a certain inductance. Also, the tracks must be wide to support large current density especially on the low voltage side. High quality factor (Q) is also needed to have high efficiency and high linearity in PAs.

In this paper, we analyze several on-chip symmetric center-tapped transformer structures utilizing the standard winding layouts. Section 2 focuses on the challenges in on-chip transformer design especially for high power RF front-ends. Section 3 describes the transformer design process and EM simulation results. On the basis of simulation results, final transformer is selected out of multiple designs. The simplified equivalent transformer model for low frequency applications is discussed in Section 4 while correlation between EM simulated and equivalent model results of the final design is shown in Section 5. Finally, the paper is concluded in Section 6.

2. Challenges in On-chip High Power Transformer Design for RF Front-ends

Several factors restrict the application of on-chip transformers in RF circuits. Firstly, the magnetic core that is normally used in electrical circuits to confine magnetic flux is not applicable because RF transformers require excellent linear response while magnetic core introduces hysteresis. Consequently, the flux leakage and capacitive coupling to the substrate as well as inter-winding capacitance deteriorate the transformer performance. Secondly, the series resistance associated with the metal windings is often substantial because the metal thickness is usually lesser than its skin depth in existing silicon IC process. The resultant current consumption and power dissipation due to the transformer are generally higher than what is required [3].

In case of a PA, a transformer must be designed to provide impedance transformation, balun operation, DC isolation and DC biasing. This biasing is provided through center-tapping which makes the use of center-tapped symmetric structures compulsory. There are several challenges in designing such on-chip transformers for RF front-ends. These challenges become more stringent for high power (~30dBm) applications and are as follows:

- The PA efficiency is dependent on transformer efficiency (η_t) which is given by [4]:

$$\eta_t = \frac{R_L / N^2}{\left(\frac{\omega L_p / Q_s + R_L / N^2}{\omega k L_p}\right)^2 . \frac{\omega L_p}{Q_p} + \frac{\omega L_p}{Q_s} + \frac{R_L}{N^2}} \tag{1}$$

  where L_p is the primary inductance, Q_p,Q_s are quality factors, k is the coupling factor and N is the turns ratio. This equation shows that high Q is needed to have high efficiency in PAs. In silicon RF circuits, the Q-factor is typically low and restricted by the metal thickness and resistivity. Q-factor can be increased by using wide and long metal windings which in turn reduce coupling and increase area.
- The different functionalities of LNA, PA and other RF circuits require different transformation networks for optimal performance. For LNA, input noise matching is desired to minimize noise figure while for PA, wide traces are often needed to handle high DC current. However, wide traces have low k-factor as coupling is on the edges only. Coupling can be improved by using multiple parallel paths or through stacking but this considerably reduces the winding inductance.
- Large inductance values require less wide but long metal paths due to which the winding resistance as well as the outer diameter increases. Hence, the overall area increases. Fig. 1 shows the graphical representation of (1) where transformer efficiency is plotted against primary inductance, L_p. The values of other parameters are given in Section 3. This figure clearly depicts that transformer efficiency is maximum only at a certain inductance. Achieving this inductance value at the desired frequency of operation is very challenging.

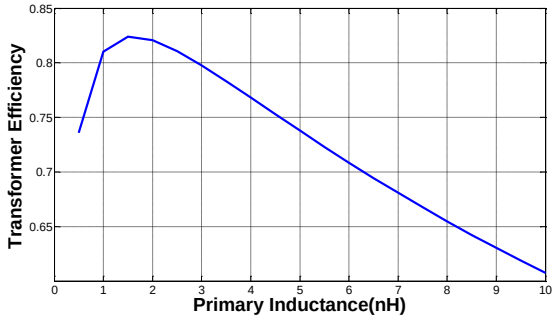


Fig. 1. Transformer Efficiency vs. Primary Inductance

3. Transformer Design for High Power RF Power Amplifiers

A. Considerations for Transformer Design

The goal of a design method for on-chip transformers is to realize the desired bandwidth and inductance with the lowest possible losses and chip area. The important figures of merit for an on-chip transformer are: k-factor (coupling coefficient), source and load impedances (including winding resistances, rp and rs), self-inductances (Lp and Ls) of the individual windings, quality factors (Qp and Qs), turns ratio, transformation ratio and area. A k-factor close to unity indicates perfect coupling and gives the widest bandwidth. It is given by:

$$k = \frac{M}{\sqrt{Lp.Ls}} \qquad \begin{matrix} \text{k=1; Perfect coupling} \\ \text{k=0; No coupling} \end{matrix} \qquad (2)$$

where M is the mutual inductance between the primary and secondary windings. Choosing an optimal inductance value is also important in on-chip transformer design especially for RF PAs as it serves two purposes: maximize efficiency as evident in (1) and provide inductance value required by the PA configuration. The value at which both these requirements are fulfilled is considered the best. Q-factors must also be high to obtain high efficiency and high linearity.

B. Transformer Prototypes

The starting point for our transformer design was manual layout in Cadence Virtuoso XL. A number of symmetric center-tapped structures were designed and EM simulated in Sonnet 13.54. Some of these transformer configurations are shown in Fig. 2. The primary winding is shown with blue lines and black lines show the secondary winding. The transformer design is characterized by turns ratio, number of turns, track width and outer diameter. We designed transformer layouts covering a wide range of geometric parameters: width 5-18μm (with stacking and/or parallel paths), 1-3 turns (turns ratio of 1:1, 1:2, 1:3 and 2:3) and outer diameter 150-750μm. This resulted in multiple transformer layouts. The standard input and output impedances of 50Ω were chosen for simulation. The transformers were designed in 0.13μm CMOS technology. 4μm thick metal with very low sheet resistance was used for the coils, and thinner metals were stacked to form the underpasses. The 300.1μm thick Silicon substrate had a resistivity of about 1.502Ω-cm.

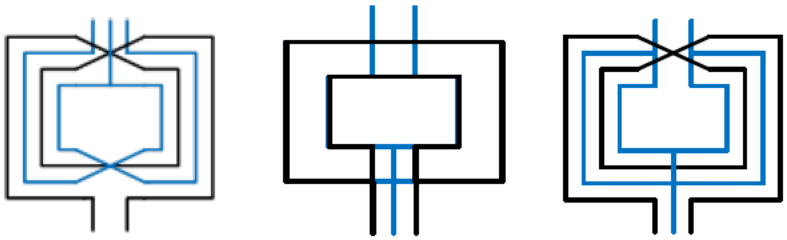


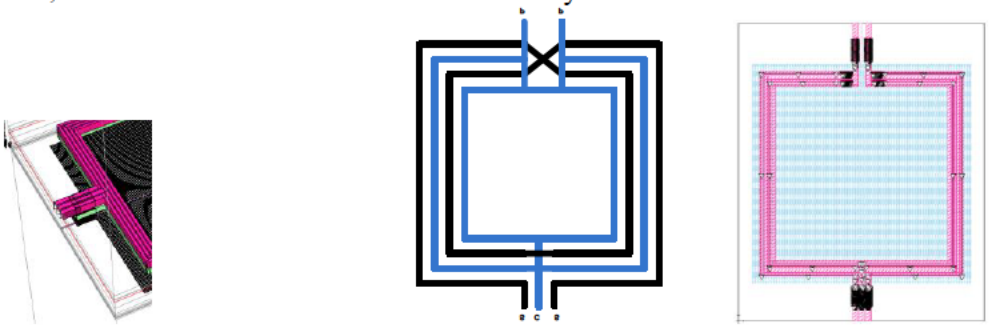
Fig. 2. (a) 1:1 Center-tapped transformer (b) 1:1 Stacked center-tapped transformer (c) 1:2 Center-tapped transformer

The first configuration was a 1:1 center-tapped transformer with two primary coils and two secondary coils, each connected in series as shown in Fig. 2(a). This configuration required wide metal tracks to sustain high current density which increased the overall size and reduced coupling. Stacking any one or both the coils improved coupling but inductance decreased substantially. Fig. 2(b) shows our next configuration. It was a 1:1 center-tapped transformer where both windings were on different metal levels and were placed over one another to improve coupling. Multiple turns in this configuration required the use of different metal layers which is not appropriate as most of the existing foundry models provide only one or two thick metals (thickness ≥3μm). Also, using lower metal layers increases the coupling to

substrate and may disturb the symmetry as well. Fig. 2(c) shows our third configuration. It was a 1:2 center-tapped transformer with two parallel primary paths and two series secondary coils. Parallel paths allowed the use of less wide tracks as current in each path reduced, thereby, improving coupling. The decrease in primary inductance can be compensated by keeping less track width and increasing area (path length). Our final transformer design with 1:2 turns ratio was based on third configuration and is shown in Fig. 3. Symmetric primary and secondary metal windings, equally spaced at 5µm and each residing on same metal layer (4µm thick, 10µm wide), were used. The primary winding was center-tapped with two parallel paths while the secondary winding had two turns connected in series as shown in Fig. 3(b). The secondary winding was also stacked with another thick metal (3µm thick, 10µm wide) to further improve coupling. On the downside, the inductance of secondary winding reduced but this did not yield any adverse effect on our PA design. The simulation results of some of our best designs based on above three configurations are reported in Table I. Our final design is reported at no. 3 and is highlighted.

C. EM Simulation of Final Transformer Design

Sonnet is a 3D EM solver from Sonnet Software, Inc. It can give accurate results in a wide frequency range given that the simulation parameters are chosen appropriately. Hence, it can be used easily to design accurate transformers. Fig. 3(a) and (c) show the Sonnet setup for our 1:2 step-up transformer. 5 port model and built-in equation macros were used to perform our analysis. Simulation results indicate primary inductance, Lp, of 1.654nH and secondary inductance, Ls, of 5.608nH at 1.8GHz. Fig. 1 shows that transformer efficiency is maximum at Lp~ 1.5nH. Moreover, our PA design also required an inductance of ~1.5nH. Hence, this transformer gave us our required inductance and maximum efficiency with a total area of 730 X 730µm^2. The quality factors, Qp and Qs, were 13.99 and 13.41 respectively. The series winding resistances, rp and rs, were 1.24Ω and 3.08Ω respectively with a coupling co-efficient, k, of 0.756 at 1.8GHz. This transformer showed a return loss, S11, of approximately -2.15dB and S21 of -5.309dB at 1.8GHz as demonstrated in Fig. 4. This S11 is suitable for our application as it yields an input resistance of approximately 28.36Ω and requisite inductive reactance. Fig. 5 shows top-level 2D and 3D views of current density. As evident in Fig. 5(c), corners of each winding hold minimal current. Hence, these corners can be chamfered without any adverse effect on results.



(a) (b) (c)

Fig. 3. (a) 3D view of 1:2 step-up center-tapped transformer (b) Winding diagram (c) Top level 2D view

Table 1: Transformer characteristics at 1.8GHz

S.No.	L_p (nH)	L_s (nH)	r_p (Ω)	r_s (Ω)	Q_p	Q_s	k	N (turns ratio)	$n=\sqrt{L_s/L_p}$	Area (µm^2)	Type
1	1.691	1.737	1.88	1.84	1.66	1.67	0.861	1:1	1:1.01	750 X 750	Fig. 1(b)
2	0.54	1.56	0.77	2.01	4.717	5.217	0.63	1:2	1:1.7	314 X 314	Fig. 1(c)
3	1.654	5.608	1.24	3.08	13.99	13.41	0.756	1:2	1:1.841	730 X 730	Fig. 1(c)
4	0.51	4.73	0.47	4.94	5.8	5.12	0.724	1:3	1:3.045	503 X 503	Fig. 1(c)
5	2.125	2.905	2.6	3.5	4.56	4.657	0.707	2:3	1:1.168	503 X 503	Fig. 1(a)
6	3.46	5.955	3.44	3.5	10.31	13.37	0.805	2:3	1:1.31	452 X 452	Fig. 1(a)

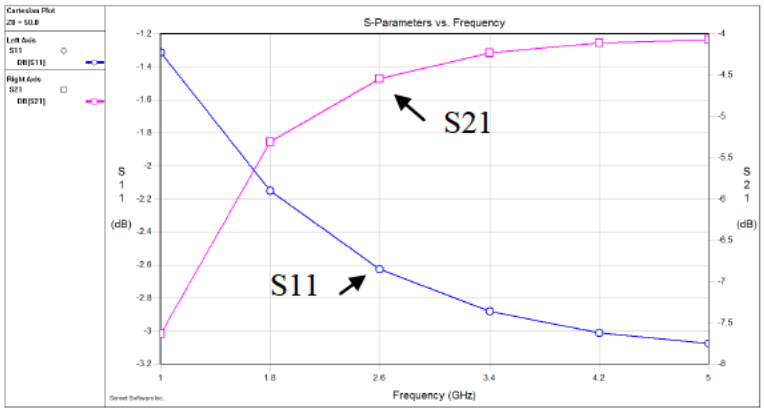
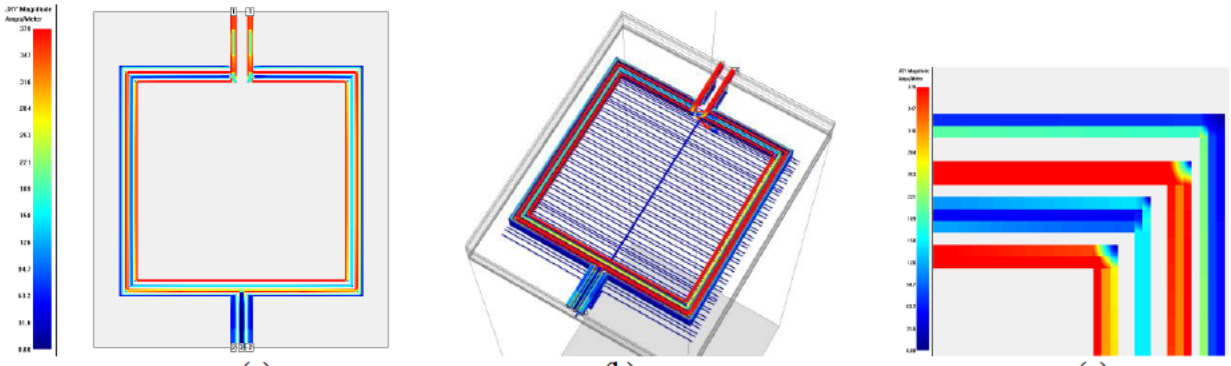


Fig. 4. S11, S21 vs. Frequency Plot

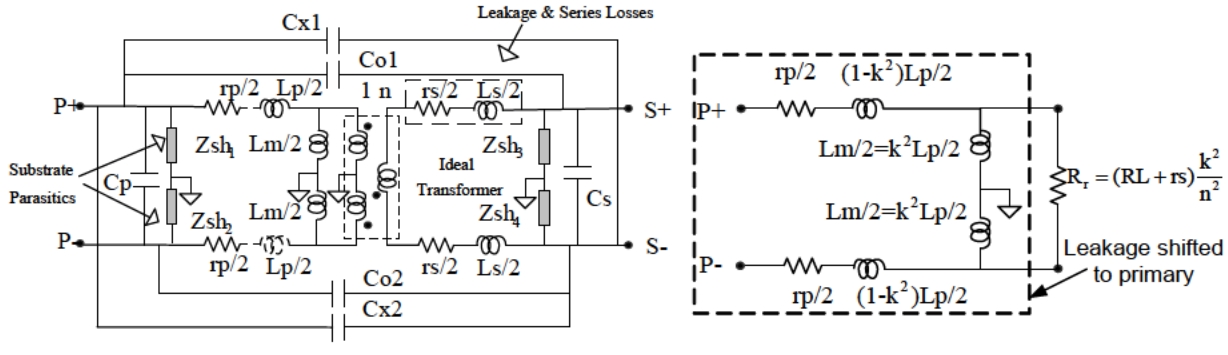


(a) (b) (c)

Fig. 5. Current Density (a) Top level 2D View (b) 3D View (c) Edges showing minimal current density

4. Equivalent Model of a Transformer

A compact model for a center-tapped transformer with four independent ports (i.e. P+, P-, S+ and S-) and 1:n turns ratio is shown in Fig. 6(a) [1]. Fig. 6(b) shows the simplified low frequency model with leakages and load shifted to primary side. Inductances, Lp and Ls, represent the primary and secondary windings of the transformer. Resistors, rp and rs, placed in series with the winding inductances symbolize ohmic losses in the windings. The center-tap at primary side is shown with a ground. The strength of the magnetic coupling between windings is specified by the k-factor.



(a) (b)

Fig. 6. (a) 1: n Compact center-tapped transformer model (b) Simplified low-frequency equivalent referred-to-primary model.

The series combination of load resistance, RL, and secondary resistance, rs, reflected to the primary side of the transformer is called Rr and may be given as

$$Rr = (RL + rs)(\frac{k^2}{n^2}) \tag{3}$$

Rr appears in parallel with the low frequency model with leakage shifted to the primary as shown in Fig. 6(b). In various applications, this model can be more simplified by grounding one or more of the ports.

5. Verification using Equivalent Transformer Model

The final transformer design was also verified using the equivalent model (Fig. 6(b)) designed in Cadence SpectreRF. The touchstone file of S-parameters generated in Sonnet 13.54 was exported to Cadence for comparison. The simulation results in Fig. 7 show good correlation, especially at low frequencies, between the S-parameters, S11 and S21, of the actual design and the equivalent model.

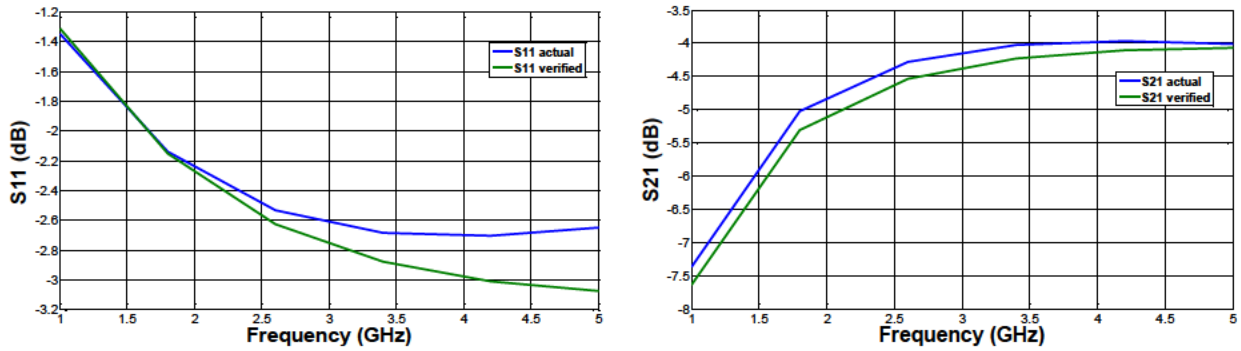


Fig. 7. Comparison of S11 and S21

6. Conclusion

A method for designing on-chip transformers suitable for RF PAs is described. Guidelines and challenges in this process are also discussed and the importance of using symmetric transformer layout for PA applications has been underscored. Multiple high power symmetric center-tapped transformers are designed in Cadence Virtuoso Layout XL using 0.13µm CMOS technology and EM simulated using Sonnet 13.54. The simulation results are confirmed using the equivalent transformer model in Cadence SpectreRF. Results show good match between theoretical calculations and EM simulation data from Sonnet. Also, comparison between our various transformer designs is made on the basis of k-factor, winding resistances, self-inductances, quality factors, turns ratio, transformation ratio and area. Post layout simulation results show that a differential Class D^{-1} PA using the designed transformer at its output provides 29dBm output power at 1.8 GHz and has an overall PAE of 52%. The fully integrated PA is taped out through MOSIS in their November 2011 run for fabrication.

References

[1] L. Gang, et al, "Fully Integrated CMOS Power Amplifier With Efficiency Enhancement at Power Back-Off," IEEE Journal of Solid-State Circuits, vol. 43 issue.3, pp. 600 - 609, March 2008.

[2] J. R. Long, "Monolithic transformers for silicon RFIC design," IEEE JSSC, vol. 35 issue.9, pp.1368-1382, September 2000.

[3] H.Y.D. Yang, J.A. Castaneda, "Design and analysis of on-chip symmetric parallel-plate coupled-line balun for silicon RF integrated circuits," IEEE RFIC Symp., pp. 527–530, 2003.

[4] I. Aoki, et al., "Distributed active transformer-a new power-combining and impedance-transformation technique," IEEE TMTT, vol. 50 issue.1, pp. 316 – 331, 2002.