Physical Modeling of a Parasitic Net Area Check (NAC) Tie-Down Diode for De-embedding

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Abstract: This paper demonstrates the measurement of the admittance of a parasitic 'tie-down' diode (also referred to as a Net Area Check or NAC diode) by the use of a through test structure. A physical model of the diode is realized and compared with the diode's extracted admittance. For verification, the diode model is used in an electromagnetic simulation (EM) of an on-chip inductor test structure and compared against the measured results. Additionally, the inductor simulation without the diode model is compared against measured results with the on-chip inductor de-embedded from the parasitic diode. The two comparisons demonstrate the diodes use in both predictive EM simulation and measurement de-embedding. The Sonnet software package is used for all EM simulations while Agilent's ADS simulator is used for further S-parameter simulations. The test structures discussed are fabricated in a 130nm RF CMOS process.

Keywords: Sonnet, Modeling, Diode, Test Structures, Through De-embedding

1. Introduction

The desire for affordable, high bandwidth wireless communications necessitates fully integrated systems on chip (SoC). These compact systems often include radio frequency (RF) transceivers alongside lower frequency digital and analog circuits. To decrease cost, SoCs are fabricated in processes designed to meet the needs of high density digital integration, often to the detriment of RF performance. To maximize RF circuit performance of an SoC, several factors must be accounted for in the design flow. These factors include digital process characteristics, such as low substrate resistivity, which lower the quality of RF passives and require careful design to overcome [1]. Additionally, sensitive RF components must be shielded from the digital systems on chip to decrease unwanted coupling and parasitic. Due to these reasons and the close proximity of RF components to digital and analog circuits, electromagnetic (EM) simulation of high frequency passive components and interconnects is crucial in ensuring the desired performance.

When combining digital and RF circuits on an SoC, a number of design rule checks (DRC) intended for the digital portions of the design are applied to the RF passives as well. Among them are checks to guard against electrostatic discharges during the plasma processing steps in fabrication [2]. To prevent these discharges from damaging transistors, a small 'tie-down' diode is required. This diode, often referred to as a Net Area Check (NAC) diode, is attached to metal wires connecting transistors and carries

away the excess charge built up during fabrication. While this diode is essential, it can often interfere with the accurate design and modeling of RF components. In Section 2, the admittance of a tie-down diode is extracted through measurement and then modeled using ideal components. In Section 3, the measured diode is then used in the simulation of an RF inductor test structure and compared back to measured results. All EM simulations are performed in the Sonnet environment.

2. Tie-down Diode Extraction and Modeling

A. Diode Admittance

To measure the effects of the tie-down diode, a 2-port, through de-embedding structure is created and used for on wafer probing, as shown in Fig. 1. The test structure is designed symmetrically with the diode added to only one signal pad by a transmission line and via. In characterizing the test structure, a lumped pi-model is used to account for the impedances of the layout [3]. The transmission line connecting the two signal pads is viewed as a series impedance with the pads modeled by the shunt elements shown in Fig. 2. The diode admittance can be extracted from the test structure measurement through symmetry. By assuming the admittance, *Y1,* in Fig. 2 is equal to the admittance *Y2*, one can then extract the Y_D from the Y-Parameters of the structure. This is shown in Equation 1.

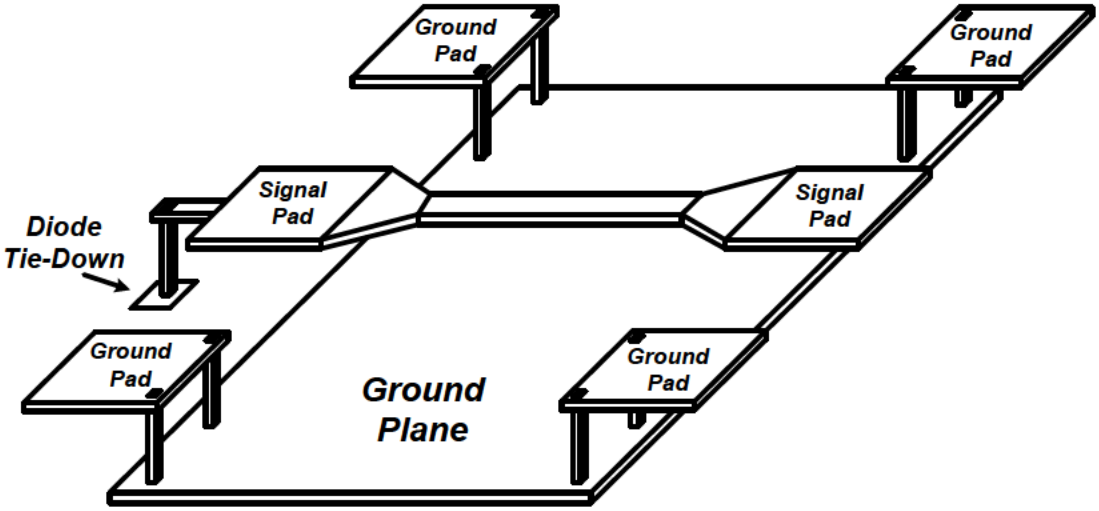

Fig. 1. Through de-embedding structure with a 'tie-down' diode added to one signal pad.

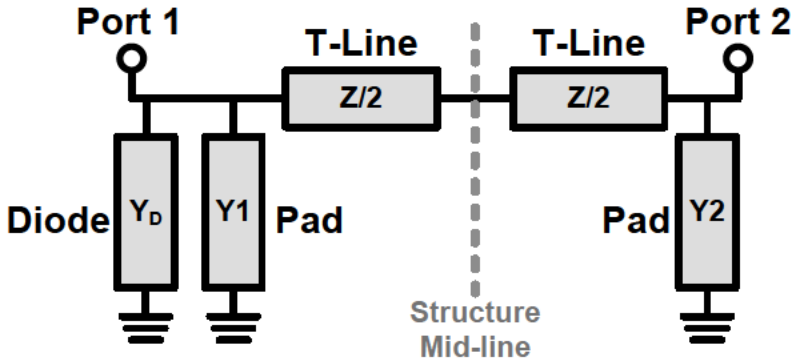

Fig. 2. The pi-model equivalent of a through de-embedding structure shows the asymmetry created by the 'tie-down' diode.

$$Y_D = Y_{11} - Y_{22} \tag{1}$$

B. Diode Model

After the extraction of the diode admittance from the Y-Parameters of the through test structure, Y_D can then be used to construct a model diode. From the layout of the diode, a five-element model is built as depicted in Fig. 3. The top resistor in the model is used to account for the resistance presented by the via metal. Since the via travels from the top metals, through several metal layers, to the substrate, this resistance is not negligible. The second and third components of the model are the contact resistance and capacitance. These two parts of the model can be ignored for lower frequencies, but above ~15GHz they are deemed necessary to accurately model the system. The fourth part of the model is the large junction capacitance. This capacitance is a function of the surface area of the diode and is the dominant component at lower frequencies. The final part of the model is the substrate resistance. As seen in Fig. 3, a model consisting of only the junction capacitance and resistive losses is valid until ~15GHz, with the full model valid to the measurement limit of 50 GHz.

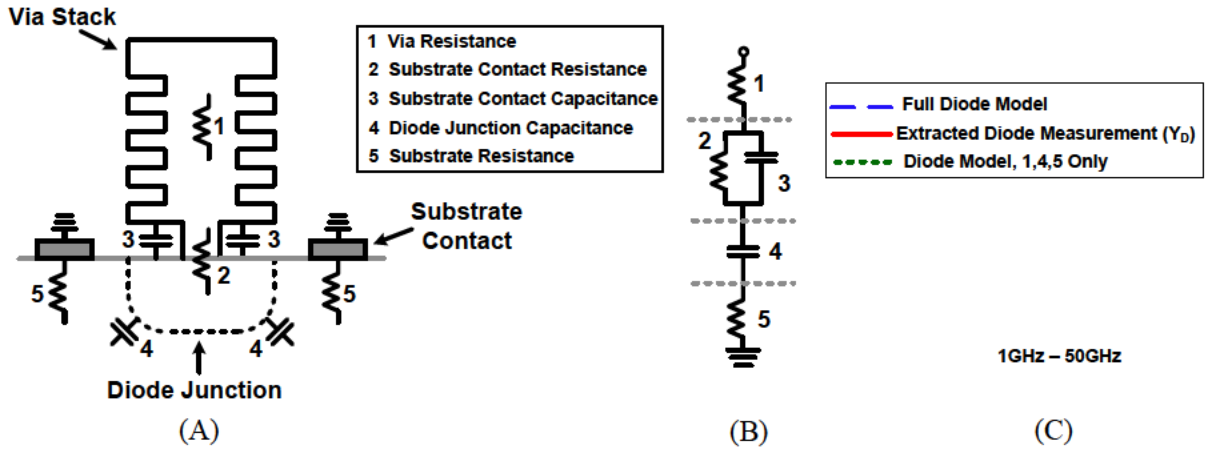

Fig. 3. The tie-down diode model. (A) Cross section of the diode layout. (B) Diode circuit model. (C) Diode model comparison showing the admittances of the extracted diode, the full diode model, and a simplified model.

3. EM Simulation and Comparison

A. EM Simulation with Diode Model Compared with Measurement

In addition to the on-chip through structure, an inductor test structure is also fabricated. The on-chip inductor has a tie down diode constructed identically to the diode in the through test structure. The matching diode layout allows the model to be used in conjunction with an EM simulation to verify the model's accuracy. The EM simulation is made of three parts with the body of the simulation layout shown in Fig. 4. The second part of the simulation layout is the back of the probe pads (not shown). The test structure layout was separated in this way to account for the RF probes contacting the pads at their center. The final part of the simulation is the diode model in Fig. 3. The individual parts of the structure are then cascaded together and simulated as a whole. Fig. 5 shows a block diagram of the final simulation organization.

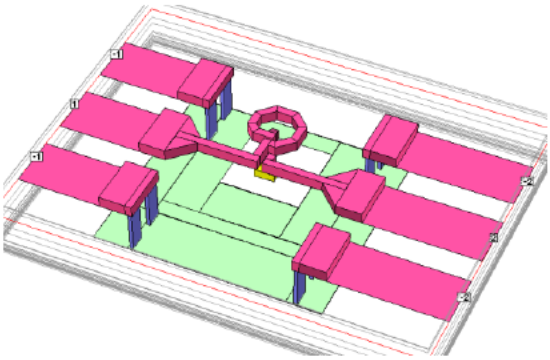

Fig. 4. Sonnet layout of a fabricated inductor test structure. The contact pads are split into two sections (back sections not shown) and simulated separately.

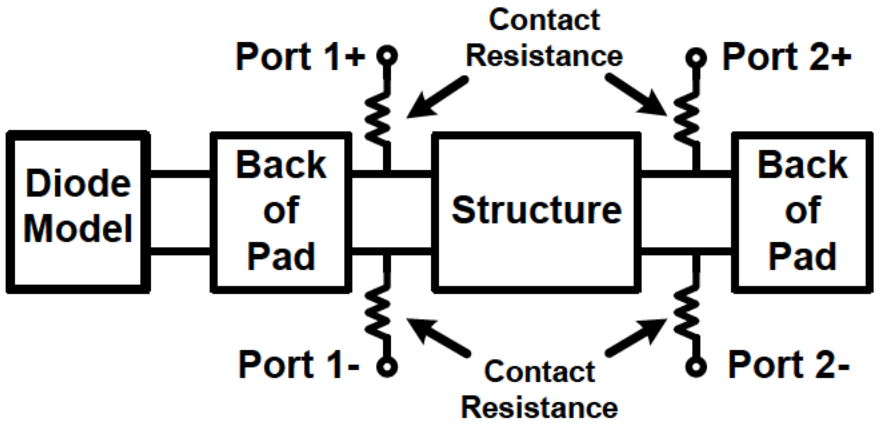

Fig. 5. Simulation of the inductor test structure. The diode model used is represented above in Fig. 3. The inductor structure and the back of the pads are EM simulated in Sonnet with their S-Parameters cascaded as shown above

Fig. 6(A) shows the S-parameters for this simulation. Due to the diode's presence, the reflected signals, S_{11} and S_{22}, are not symmetrical even though the structure itself is largely symmetrical. The asymmetry of the reflected waves shows the impact of the diode is confined to S_{11} and S_{22} and is not evident in the transmission through the structure. The EM simulation with the diode model shows close matching to the measured data at lower frequencies. However, the S_{11} and S_{22} of the model begin to diverge from the measured data at frequencies above ~35 GHz. At 50 GHz, the measured S_{11} magnitude is -12 dB while the simulated magnitude is only -8dB. The S_{12} and S_{21} data matches over the entire measured frequency range with a maximum deviation of 0.45 dB.

The match between the simulated and measured S-Parameters indicate that the model can be used effectively for predicting the behavior of the 'tie-down' diode. Especially below ~35 GHz, RF inductors, transmission lines, and interconnects with attached 'tie-down' diodes can be accurately modeled.

B. EM Simulation Compared with Diode Subtracted Measurement

A second comparison between simulation and measurement is made. For this comparison, the diode admittance is subtracted from the Y_{11} of the measured inductor data, effectively removing the diode from the inductor test structure. This data is compared to an EM simulation without the model diode. As expected, the measured data with the diode removed is now effectively symmetrical because of the manipulation (Fig. 6(B)). The simulated and measured transmission through the inductor matches well

across the measurement frequencies as before. The reflections, S_{11} and S_{22}, of the simulation match to higher frequencies than the previous case, but begin to diverge at ~40 GHz. This comparison indicates that the diode model is also useful for mathematically removing the effects of the diode from a test structure after the measurements have been taken.

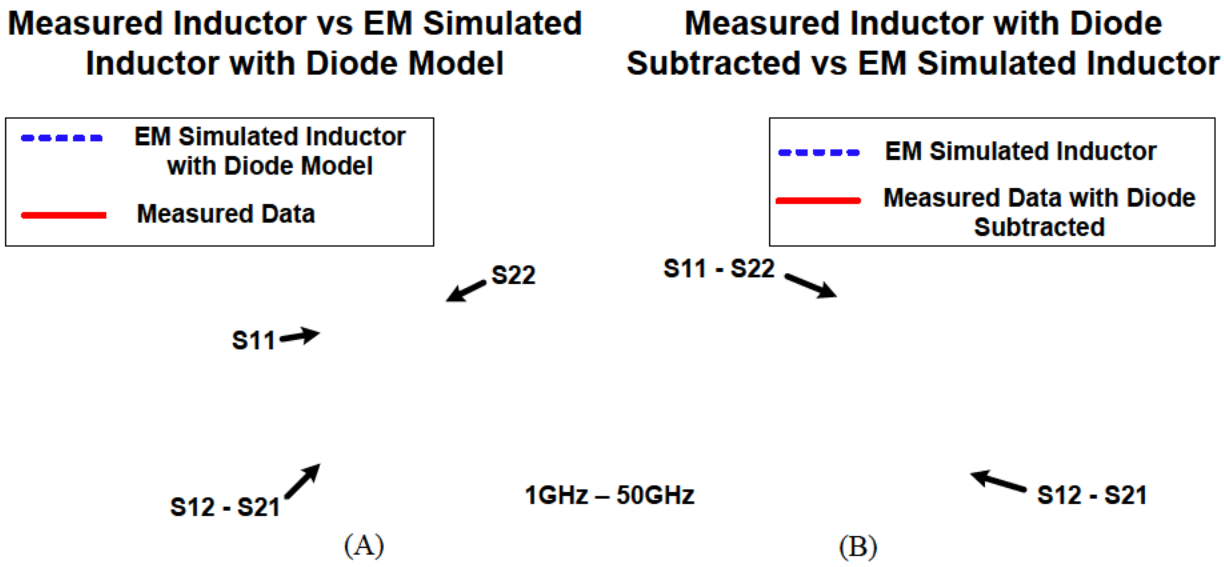

Fig. 6. EM simulated inductor compared with measured results. (A) EM simulated inductor with diode model compared with measured results. (B) EM simulated inductor compared to the measured inductor test structure de-embedded from the diode.

4. Conclusions

In this paper, the effects of a parasitic tie-down diode are extracted from a through test structure. The diode's admittance is obtained and a physical model for the diode is realized. The physical model matches the extracted diode admittance across the measured frequency range, and the model is used in conjunction with an EM simulation of an inductor and compared to measured results. Since the two data sets compare well, the diode model can be used to accurately predict the tie down diode in simulation. Additionally, the diode admittance is used to subtract the diode effects from measured results showing the model can also be used to de-embed various structures from the diode after measurements are taken.

References

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