RFIC Test Board Design and Modeling using Sonnet™

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Abstract: Test or prototype boards are used extensively in RFICs to integrate monolithic microwave integrated circuits (MMICs), bypass networks for biasing, external matching networks, and connectors. In the design and layout of the test boards, accurate EM simulation is sometimes only considered as an afterthought. In this paper, a design methodology for testboards including EM effects such as parasitics and coupling using Sonnet is given. A hybrid simulation is proposed whereby an EM model is used in a circuit simulator at RF frequencies (> 100 MHz) while an equivalent circuit model is used for envelope frequencies and DC. Case studies are included to show effects such as slot line modes and identify resonance behavior.

Keywords: MMICs, Microwave Circuits, Modeling.

1. Introduction

The fabrication of RFIC's requires the integration of several components onto a single board. The main component is the MMIC, which includes most of the active circuitry. Surface mount components (SMTs) are also used for tuning and to provide bypassing of the bias networks. Bond wires and microstrip lines are used as interconnects. Due to this complexity, multiple inter-operable simulation platforms are required to design and model these circuits. Unfortunately, the prototype or test board design is often an afterthought and is prone to effects such as over-moding due to the presence of CPW, slotline, and microstrip propagation modes. In addition, other effects such as coupling and parasitic inductance and capacitance due to bond wires and solder pads must also be considered.

Sonnet™ [1] is a powerful EM simulation tool that can be used in the design of design test boards. Sonnet allows internal ports to be included which are then used in a standard circuit simulator to include effects of SMTs, bond wires, and the MMICs. This is advantageous in that the designer can layout a test board, EM simulate it, and then optimize the SMT values for optimum performance. This procedure can be carried out using only one or two EM simulations of the test board and is similar to tuning methods [2]. Sonnet uses co-calibrated ports in the interior of the circuit. During the simulations, these ports are de-embedded so that the coupling between the ports is removed. This allows for external components like chip inductors, capacitors, and resistors to be connected to the circuit outside of the Sonnet environment. This is useful in the test board design because it allows a wide range of SMTs having different values from different vendors to be considered in the test board design.

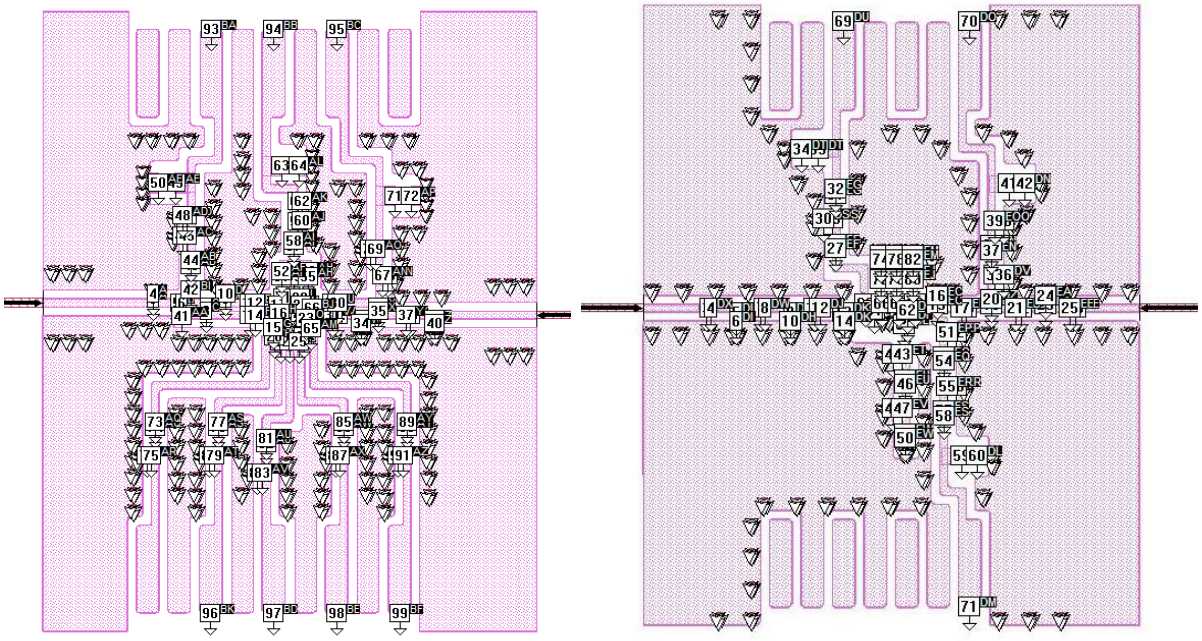
Test board design can be easily over-constrained in that the SMTs, MMIC die, bond wires must all be accommodated. As a result, the effects of parasitics and coupling can result in unwanted resonances. These effects cannot always be detected using the built-in or "canned" models in circuit simulators.

2. Testboard Specification and Design

The prototype boards have 3 metal layers and use Roger 4350 between the top and inner metal and FR4 between the inner and bottom metal. The top, inner and bottom metal layers are made of copper. The inner metal layer acts as an RF ground. Plated through via holes connects the top metal to other metal layers. Top and bottom metal are exposed in certain places with immersion gold finishing for wire-bonding and soldering purposes. Half-ounce copper (Cu) with 18 μm thickness is used for all three metal layers. Gold finishing is sputtered on top of nickel (Ni) layer, which is adhesive to copper. The substrate material used between top metal and inner metal is the Roger 4350 with 10 mil thickness with dielectric constant (ε_r) of 3.48, and loss tangent ($tan\ \delta$) of 0.004. Between the inner metal and back metal, FR4 is used as the support layer with 42 mil or 32 mil thickness, dielectric constant (ε_r) of 4.5, and loss tangent ($tan\ \delta$) of 0.03. Initially, layout design of prototype board was done using AutoCAD. The layout was imported to Agilent's Advanced Design System (ADS) 2008, which was then converted to Gerber file (standard file format for PCB fabrication).

3. Electromagnetic Simulations of Model Testboards

Sonnet™ release 12 was used to perform full-wave EM analysis including the parasitic effects from prototype board for use in the circuit simulations. The top metal layer is the most complex structure. Therefore, only the top metal layer was simulated to reduce the memory requirement of the simulation. The EM simulations were performed at frequency between 0.1 GHz to 4 GHz with 0.1 GHz steps. The field simulation was drawn with cell size 0.1 mm × 0.1 mm in a box size of 60 × 70 cells as shown in Figures 1(a) and 1(b). Ground connections were included using square vias are, also, shown. The simulation also includes the characteristics of Roger substrate as well as the copper layer (thickness and conductivity). Standard ports and co-calibrated ports were included in the simulation so that the Touchstone format data produced by the field simulator can be integrated in the schematic simulation. There are 97 co-calibrated ports (internal ports) included in testboard #1 simulation and 83 co-calibrated ports (internal ports) included in testboard #2. Testboard #1 is used for a reconfigurable power amplifier and testboard #2 was used for a distributed amplifier [3-4].



(a) Testboard #1 (b) Testboard #2

Fig. 1. Prototype board layouts in Sonnet™ for testboards 1 and 2.

Figure 2 shows the hybrid EM-circuit simulation for a reconfigurable power amplifier [3]. In addition to the SMTs and bond wires, this test board, also, has two MMIC die [3]. The Touchstone data from prototype board's EM-simulation was integrated in the ADS schematic simulation using the data file tool. The other parasitic effects that are not accounted for in the S-parameter block, such as wirebonds, bondpads, and vias between top metal to bottom metal, are included using the built in ADS model.

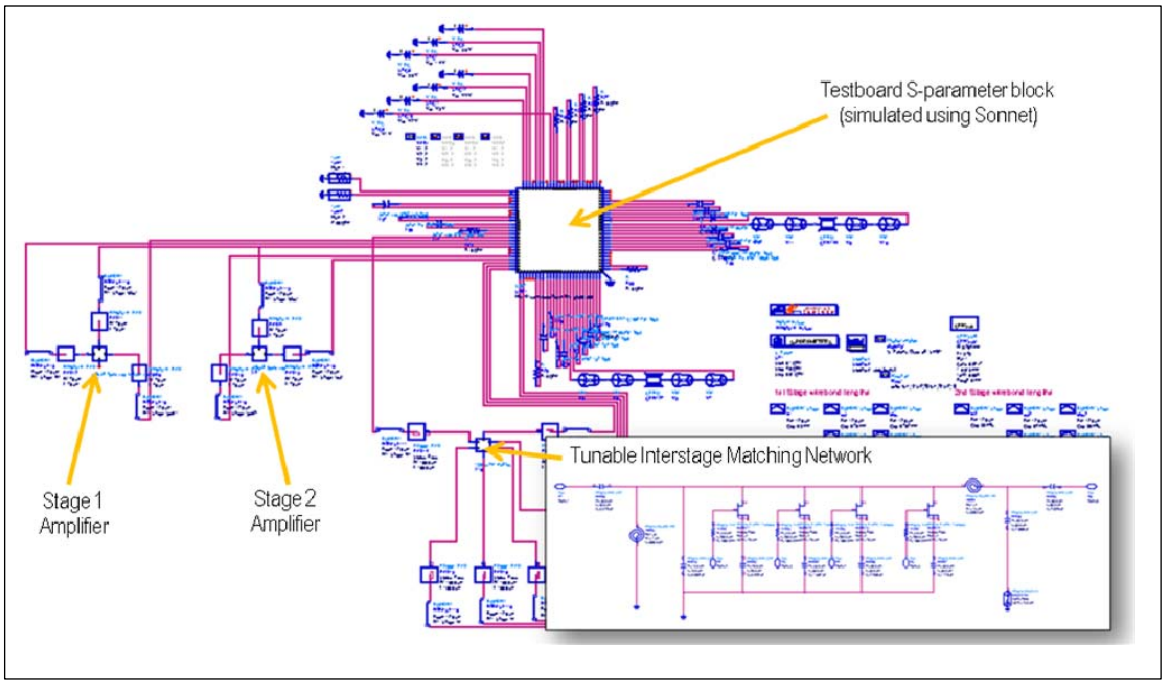


Fig. 2. Hybrid EM-circuit simulation for reconfigurable PA.

The prototype test boards were modeled using two methods: 1) CPW model available in ADS and 2) full-wave electromagnetic simulator in Sonnet™. Figure 3 shows the circuit simulations of the reconfigurable power amplifier using CPW model in ADS and the EM simulation to model the testboard parasitic effects. For the designs that operate at a lower frequency, the simulation using CPW model and EM-simulated model do not show any significant difference. However, at a higher frequency operation (f_o > 1 GHz), these models show different responses and begin to diverge. As shown in Figure 3, above 0.5 GHz, the $S_{11,}$ S_{22}, and S_{21} response using the hybrid EM-simulated model is closer to the measured data. The hybrid EM model accurately predicts the drop in S_{11} at about 1 GHz and the nulls in S_{22} at 1.1 GHz and 2.3 GHz. The measured peak in S_{11} at 2 GHz is also more accurately predicted using the hybrid EM model.

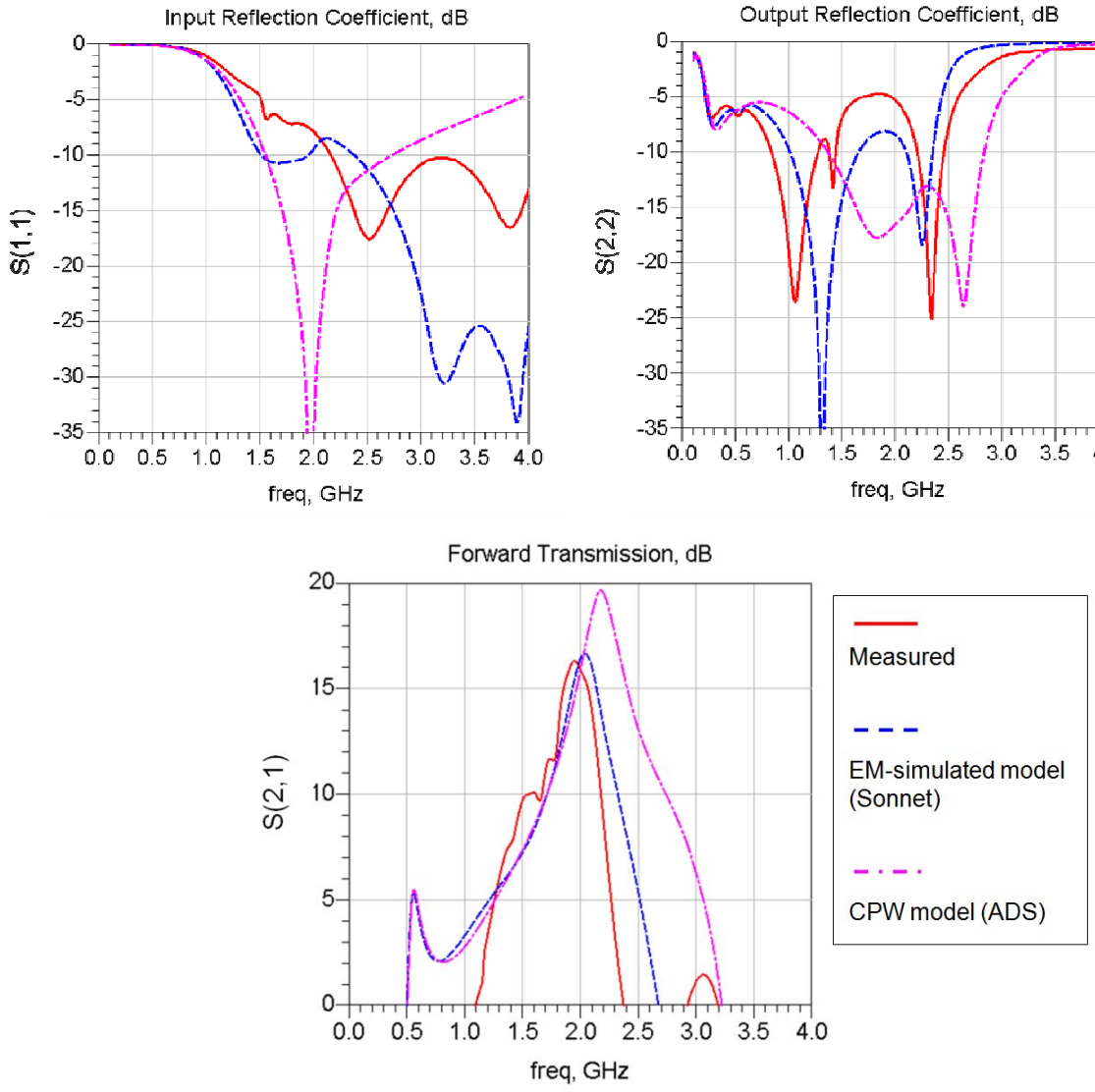


Fig. 3. CPW model vs. EM-simulated model for prototype testboard #1.

For the second case, a prototype test board was developed for a distributed amplifier [4]. The measured vs. simulated responses are shown in Figure 4. Again, the agreement with the built-in models below about 0.5 GHz is quite good. At higher frequencies, the hybrid EM model shows much better agreement with the measured data. The hybrid EM model accurately predicts the nulls in S_{11} measured at 1.7 GHz and 3 GHz and S_{22} at 0.6 GHz. The agreement with the measured S_{21} is also much closer using the hybrid EM model.

The transmission lines used on the prototype boards were designed as a grounded CPW structure (grounded metal on the sides of the lines) wherever possible. For the grounded CPW structure, both microstrip and coplanar waveguide modes are excited. However, at the center of the prototype board, wirebond connections between the metal runner to the bondpads on the MMIC die and cause the CPW mode to be discontinuous. This discontinuity in the transmission line model of the prototype board is one of the differences between the simulation using CPW-model and the hybrid EM-simulated model.

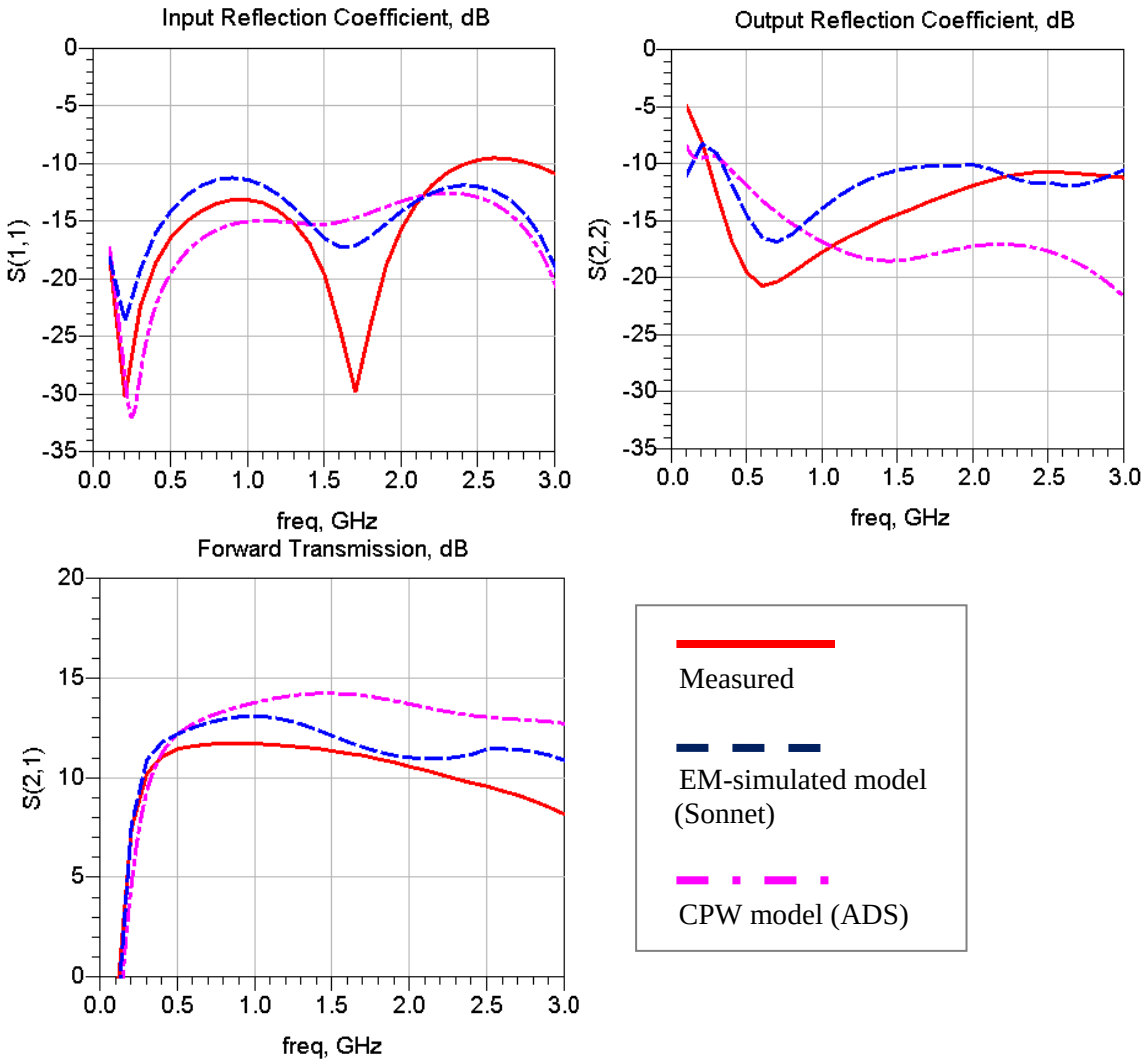


Fig. 4. CPW model vs. EM-simulated model for prototype testboard #2.

4. Discussion

The testboards discussed in the previous section were simulated to investigate the presence of any possible slot line modes in the CPW grounds. These modes are simulated by connecting the input and output lines so that the input and output becomes a continuous through line.

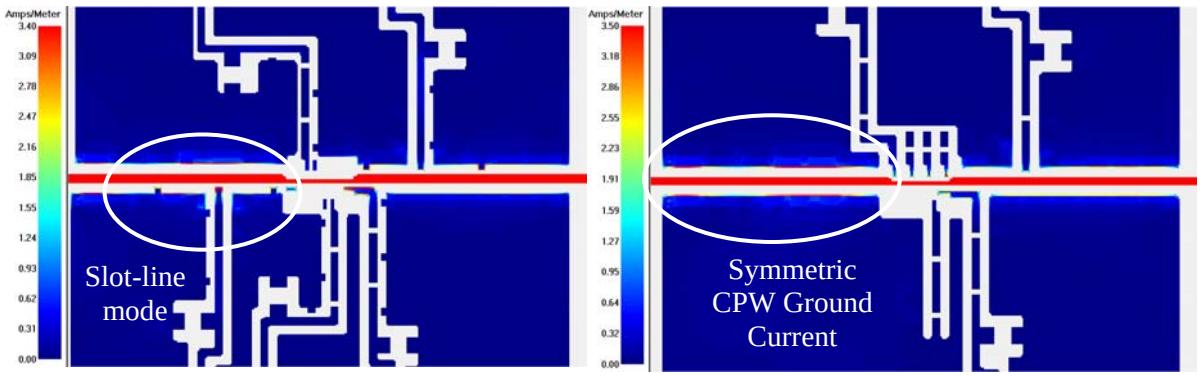


Fig. 5. Simulated current distribution at 8 GHz for testboard #2 versions 1 and 2.

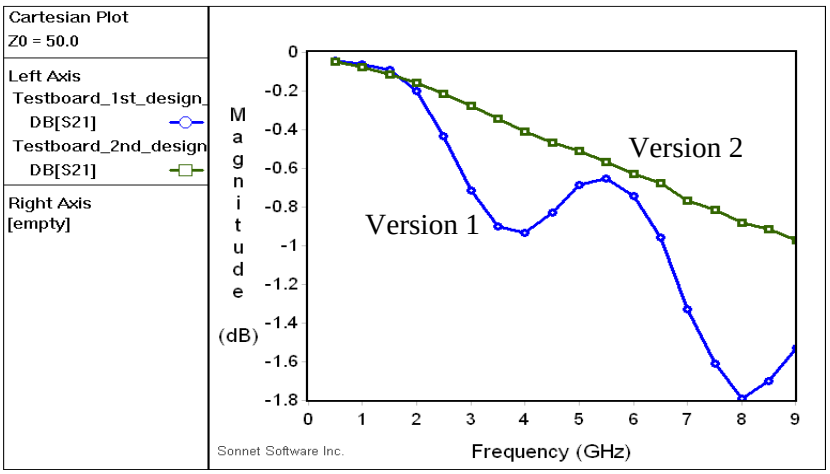


Fig. 6. Simulated S_{21} testboard #2 versions 1 and 2.

Figure 5 shows the simulated current distributions for two versions of the testboard used in testboard case #2 at 8 GHz (see Figure 1(b)). Figure 6 shows the corresponding simulated transmission coefficient, S_{21} through both versions of the testboard. It is interesting to note the variation in S_{21}. In version #1, slot line type modes can be observed at 4 and 8 GHz. In version #2, the layout was modified to eliminate these modes by removing an input feed line resulting in a symmetrical current distribution in the CPW grounds. The resulting S_{21} decays monotonically.

5. Conclusions

In this paper, Sonnet is used to analyze test or prototype boards for RFICs. Inclusion of internal ports into the test board simulation allows external components like SMTs and bond wires to be included for optimization while minimizing simulation time. Below 0.5 GHz, the equivalent circuit model and hybrid-EM model match the measurements well. Above 1 GHz, the hybrid-EM model compares better than the equivalent circuit CPW model. Above 2 GHz, the presence of slot line modes in the testboard can be found.

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