Sonnet in RF Power Amplifier Design

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Abstract: Planar electromagnetic simulator Sonnet has been used to identify the source of the non-uniformity in current distribution for parallel-connected transistors for high power applications at HF (3-30MHz) range. S-parameters and current distribution of the main board where resonators and transistors are connected are obtained with Sonnet and used in the time-domain non-linear circuit simulator, Pspice, for RF power amplifier simulation. Source current distribution for individual transistors in conjunction with overall amplifier simulation has been used to identify the hot spots for amplifier when it is terminated with matched load and open load under rated power. It is shown that planar electromagnetic simulator, Sonnet, can be used to identify the non-uniformity in source current distribution among transistors in RF power amplifiers.

Keywords: Sonnet, Planar, Electromagnetic Simulators, Non-linear, Circuit Simulators, Pspice.

1. Introduction

RF/Microwave engineering in this era requires design and implementation of components and systems with highest efficiency in cost and performance. This requires design and simulation of components before implementation to reduce the associated engineering error and cost and expedite the design process.

Planar electromagnetic simulators have been widely used to design and simulate RF/Microwave devices at the component level [1-3] whereas non-linear circuit simulators are commonly used to design and simulate power amplifiers using lumped or simple distributed models. Non-linear circuit simulation can be done using harmonic balance technique with the application of Krylov subspace methods in frequency domain or non-linear differential algebraic equations using the integration methods, Newton's method or sparse matrix solution techniques in time-domain [4-6]. Time domain non-linear circuit simulators are preferred over harmonic balance based non-linear circuit simulators because they provide transient response of the non-linear circuits using large signal equivalent models.

Although use of electromagnetic simulators and time domain non-linear circuit simulators are common practice in RF/Microwave engineering design, it is to be noted that they are not frequently used together. As a result, electromagnetic effects including coupling between traces and leads, parasitic effects, current distribution, radiation effects, etc. cannot be observed in an amplifier simulation when only non-linear circuit simulator is used. This is mostly due to requirements on expertise in component design, system design, and use of planar electromagnetic simulators in conjunction with time domain circuit simulators.

In this paper, we characterize the RF power amplifier to determine the uniformity in source current distribution among the active devices when the amplifier is terminated with loads having standing wave ratio ranging from a matched load to open load, VSWR =1 to ∞. This is accomplished by modeling and simulation of the boards that transistors and resonating inductors are connected with planar electromagnetic simulator, Sonnet, and then embedding them into non-linear time-domain circuit simulator, Pspice using their broadband equivalent models that are obtained by S-parameters. RF amplifier operating at the HF range and capable of delivering over several kilowatts to a matched load is simulated and characterized to identify the current distribution among its transistors for this purpose. The simulation results for the complete system showing the amplifier response and current distribution for each transistor when amplifier is terminated with various loads are presented.

2. Simulation of Current Distribution for Each Active Device

In this section, the main board that the transistor source leads and the resonating inductors are connected is simulated using planar electromagnetic simulator, Sonnet V12.56. The layout of the board is illustrated in Fig. 1.

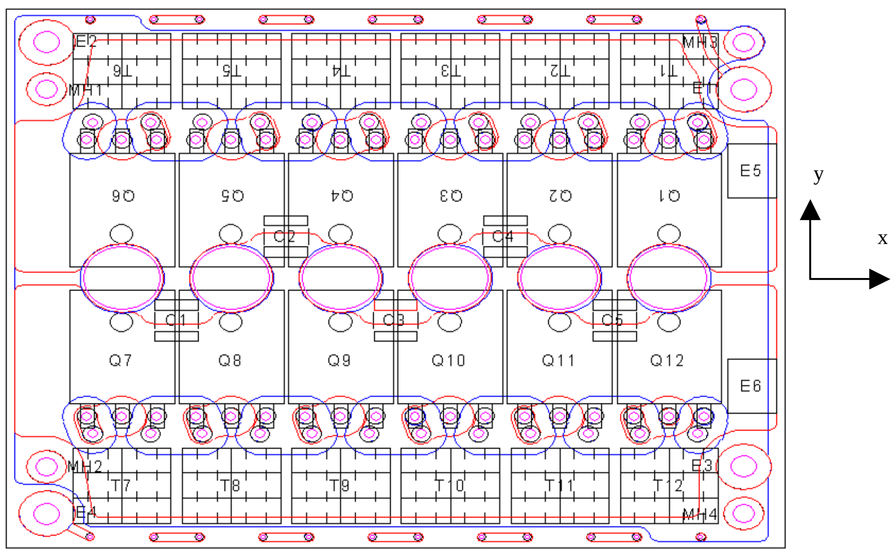

Fig. 1. The complete layout of the board.

Since the structure is symmetrical, the simulation of the board can be performed only for the half section with Sonnet. This will shorten the required simulation time. The simulation for the complete board then can be obtained with the edition of the second symmetrical section using the existing results. S-parameters can be used to model the complete board as a block and the block that is modeled by Sonnet can be used as a component in Pspice. The outline of the symmetrical part that is simulated is shown in Fig. 2. There are seven ports on each of the symmetrical sides. Six of the seven ports represent the ports where the source of each transistor is attached. They are defined as via ports. The seventh port is used to represent the termination point where the resonating inductor is connected. It is defined as a calibrated port. There are a total of 12 transistors in the amplifier and they work in push-pull configuration. Six transistors exist on the push side and six transistors exist on the pull side. On each transistor bank, transistors are connected in parallel to increase the power capacity of the amplifier. There is a load line network on push and pull side of the amplifier to match the source impedance to the load impedance. The push and pull side of the amplifier after the load line network is connected to an output balun with the additional required impedance matching. There are off-line and in-line filters that are implemented as part of the load line network to increase the stability of the amplifier. The amplifier configuration is depicted in Fig. 3.

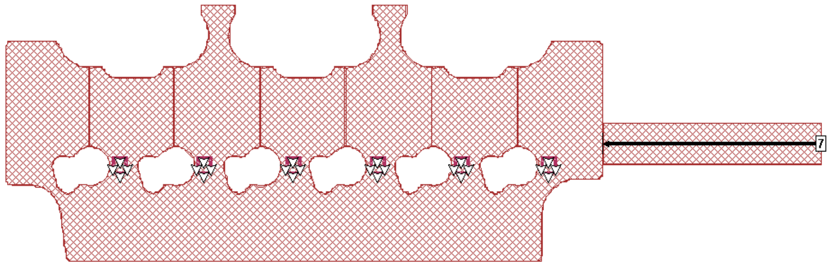

Fig. 2. The layout of the board that is simulated.

It has been observed that when the terminating load is other than a matched load, the distribution in source current becomes worse. This characteristic is dominant for open loads. The current distribution has been recorded after modeling and embedding the board in a time domain simulator, and measuring the source current for each transistor for different terminating loads.

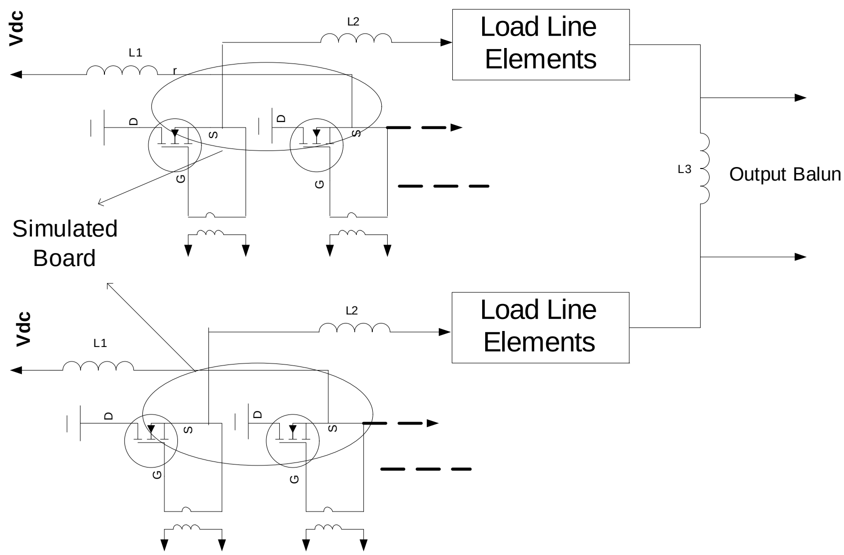

Fig. 3. Amplifier configuration.

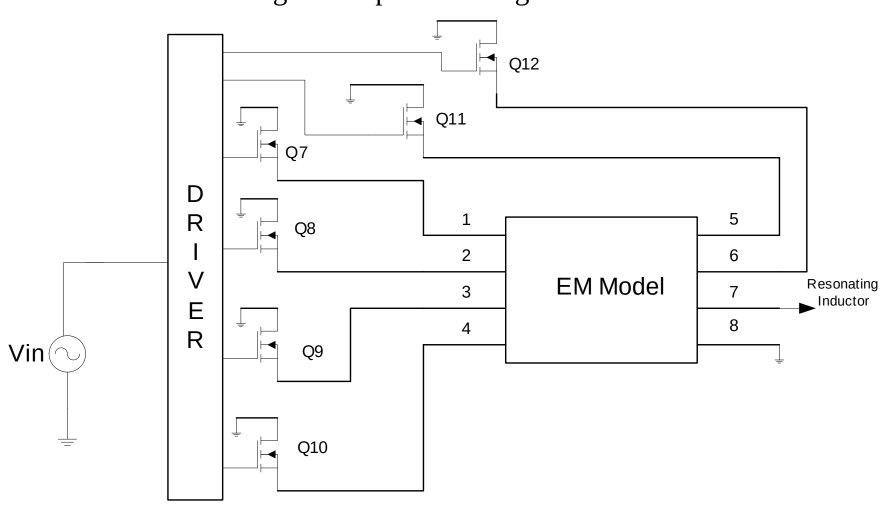

Fig. 4. Implementation of an EM model in amplifier.

3. Measurement and Simulation Results

The electromagnetic simulation of the board with Sonnet V12.56 and its current distribution has been demonstrated in Fig. 5. Based on the simulation results at the board level, the current density becomes much higher specifically around the region where transistor Q7 is connected as shown in Fig. 1. Transistor Q7 is connected to port 1 as illustrated in Fig. 4 based on the port designations in Sonnet.

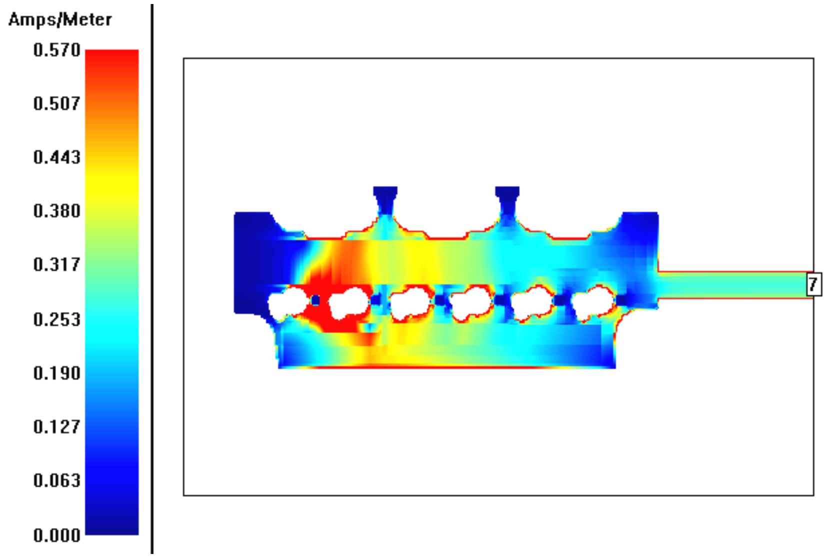

Fig. 5. Implementation of an EM model in amplifier.

After simulation of the board is completed with Sonnet to obtain its current distribution, S-parameters are used to model the board as a block that can be used by time domain circuit simulator as illustrated in Fig.4 for RF power amplifier simulation. The current distribution of each transistor for RF power amplifier when it is terminated to matched load and open load at the rated power are shown in Fig. 6 and Fig. 7, respectively.

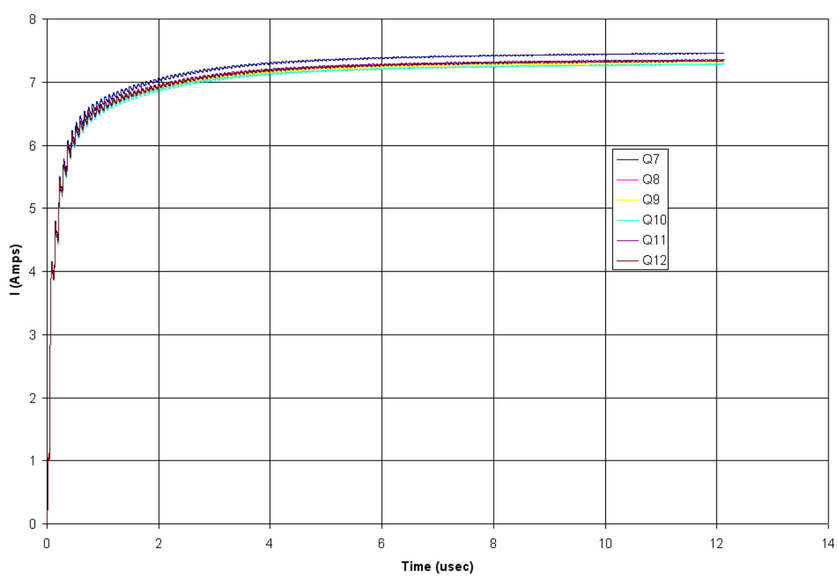

Fig. 6. Response of the transistor source current for a matched load.

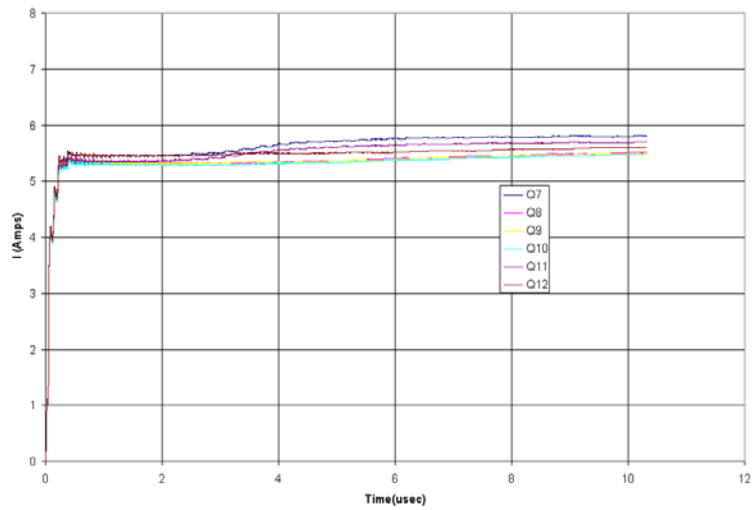

Fig. 7. Response of the transistor source current amplifier for an open load

The results that are obtained with the time domain circuit simulator confirm that the highest current distribution exists for Q7. This result aligns with the highest current density region that is obtained before by Sonnet. This indicates that the non-uniformity in source current distribution exists in the board layout design and not in the power amplifier design or transistor characteristics. As a result, the inherent problem in the board layout is reflected in the power amplifier response.

4. Conclusions

Electromagnetic simulator, Sonnet, has been used to identify the source of the non-uniformity in current distribution among transistors in RF amplifier at the HF range for high power applications. This has been found by simulating the main board with Sonnet where the transistors and the resonating inductors are connected. The simulated board then has been embedded into the time-domain circuit simulator Pspice using its S-parameters. The simulation of RF power amplifier with the modeled board has been performed. The results confirmed that the distribution of source current is worse for the transistors that are connected to the high current density regions on the main board as simulated by planar electromagnetic simulator Sonnet V.12.56.

References

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