An Efficient EM Simulation Model for ENIG Plated Metal Finishes Including Conductor Side-Wall Plating Verified With Physical Measurement from 1 to 50 GHz

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***Abstract*—A test setup is developed, measured, and modeled to examine the insertion loss effects of Electroless-Nickel Immersion-Gold (ENIG) plating on various PCB topologies from 1 to 50 GHz. ENIG plating is observed to increase insertion loss compared with unplated samples nonlinearly in a manner that generally increases with frequency. Three main topolgies are analyzed; a 0.005" (0.127 mm) thick microstrip circuit using RT/duroid® 6002 laminate, a 0.008" (0.203 mm) thick microstrip using RO4003C™ laminate, and a 0.008" (0.203 mm) thick Grounded Co-Planar Waveguide (GCPW) using RO4003C™ laminate.**

***Index Terms*—5G, Electromagnetics, ENIG, grounded co-planar waveguide, insertion Loss, metal plating, PCB characterization, PCB design, simulation.**

I. Introduction

Many PCBs have plated-metal finishes during production for corrosion prevention and durability, with Electroless-Nickel Immersion-Gold (ENIG) being a commonly used method. Conventionally, the electrical and electromagnetic effects of this plating are considered to be unknown, unimportant, or subject to *rule of thumb*. At relatively lower frequencies, e.g., up to 3 GHz, this is often an adequate approximation. However, due to the physical nature of the edge-effect, which is rooted in electromagnetic theory, the electrical behavior of metal plating can rapidly diverge from unplated metal at higher frequencies. This is of increasing importance in the 5G space due to high-frequency operation, often in excess of 20 GHz, where the effect of metal plating could seriously degrade the performance of a circuit. In this work, an experiment is developed to demonstrate the effects of ENIG clearly, a preliminary model is developed to simulate the effects, a conductivity value for Electroless-Nickel is extracted, and simulation data is compared to measurement across three topologies from 1 GHz to 50 GHz. Good agreement between simulated and measured results suggests that the technique may be used to determine potential degradation of the performance of 5G circuits before construction. Previous work has been done to study similar finishes in [1] and [2]. Notable contributions presented in this work include the addition of side-wall nickel conductor to the simulation, mild characterization of nickel-phosphorous conductivity, and measurement and simulation extending to 50 GHz, to encompass many important 5G frequencies. This paper will first overview the test and measurement setup, next the simulation setup including observations of physical phenomena, and finally compare measured and calculated data for the three topologies.

II. Test and Measurement Setup

In order to explain the test setup, it is first convenient to overview various sources that contribute to insertion loss. The total loss is defined as the summation of that occurring from conductor resistance, dielectric loss tangent, radiated resistance, and leakage, as

$$\alpha_{total} = \alpha_{cond.} + \alpha_{diel.} + \alpha_{rad.} + \alpha_{leak.} \tag{1}$$

With short lengths of very thin microstrip with little surrounding metalization, losses due to radiation and leakage are very small. As the effects of metal plating will appear in increased conductor losses, this means that the test set up will in effect need to prioritize minimizing dielectric loss. This is done in part with thin substrates, but is further optimized by using extremely low loss substrates. In this test, Rogers RT/duroid 6002 laminate and RO4003C laminate are used, each with dielectric loss tangent of 0.0012 and 0.0029, respectively.

For each topology, two sets of test circuits are produced. First, an 8" (20.32 cm) length and a 2" (5.08 cm) of transmission line. Both are produced with bare copper of the type relevant to the test, and then connectorized. Insertion loss is measured on both lengths from 1 GHz to 50 GHz, and from these measurements insertion loss per unit length (dB/in.) is extrapolated. This procedure helps to compensate for error produced in coupling with the circuit. Using the same tooling, a second set of circuits are constructed with a standard ENIG plating process and measured. The cross-section of an ENIG plated microstrip line is pictured in Fig. 1.

In this work, three test cases are considered. First, a microstrip configuration with 0.005" (0.127 mm) thick RT/duroid® 6002 laminate and smooth $1/2$ oz. Rolled-Annealed (RA) copper, to best emphasize conductor loss effects over dielectric loss and surface roughness effects. Second, a microstrip configuration with 0.008" (0.203 mm) thick RO4003C™ laminate with Electro-Deposited (ED) $1/2$ oz. copper is presented to further verify the method. Finally, a

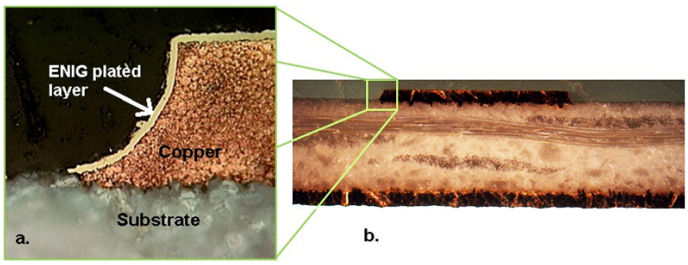

Fig. 1. A cross section of a microstrip line plated with an ENIG process. The nickel-phosphorous plating is visibly conformal. The gold coating is generally too thin to be visible [3].

Grounded Co-Planar Waveguide (GCPW) configuration with 0.008" (0.203 mm) thick RO4003C^{TM} laminate with ED 1/2 oz. copper is presented as a completely different topology with similar material characteristics.

III. Model Setup and Simulation of Physical Phenomena

In this section, both the model setup and parameters are detailed, and the models are used to observe various physical phenomena from within the circuit. This provides a physical and quantifiable understanding of the process effects, and explains the efficacy of the model.

A. General Model Setup

As the coating has been shown to be conformal as in Fig. 1, an initial electromagnetic simulation model is developed in Sonnet® Suites [5] which includes metal on all exposed sides. While the trapezoidal cross-section is not included, this is additionally possible to do and is regarded as future work. The model is drawn with a thin metal on top, with thickness equal to plating thickness, and two narrow metals on the sides, with thickness equal to the main conductor. This is pictured for microstrip and GCPW in Fig. 2. Please note that gold is not included in the pictured models for both simplicity of viewing and solving.

B. Observation of Physical Phenomena

It has been observed that the addition of ENIG plating can impact insertion loss at high frequency while having minimal effect at low frequency [3]. Conceptually, at DC the additional metal might be viewed as a second resistor in parallel, which would decrease overall resistance. As such, it is reasonable to suspect that the electromagnetic effects occurring at higher frequency are contributing to the observed behavior. A nice benefit of simulation is the ability to observe physical phenomena regarding current distributions, something that is difficult to measure directly. As such, various current distributions are simulated and viewed at different frequencies in an effort to gain a physical understanding of the plating effects.

As viewed in Fig. 3, as frequency gets higher, the current is observed to increasingly travel in the sides of the conductor cross-section, closer to the more-lossy nickel-phosphorous

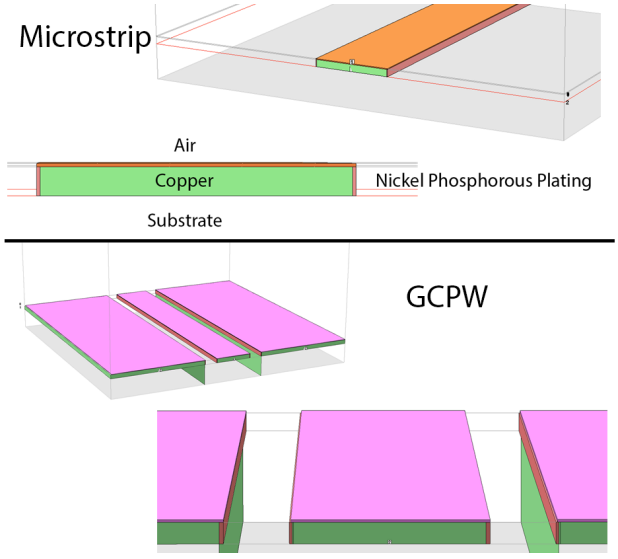

Fig. 2. Models in Sonnet including the nickel-phosphorous plating as being conformal on exposed surfaces of the main copper conductor. The sidewalls are composed of thick metal with the conductivity of nickel-phosphorous. Microstrip (Top) and GCPW (Bottom) are pictured.

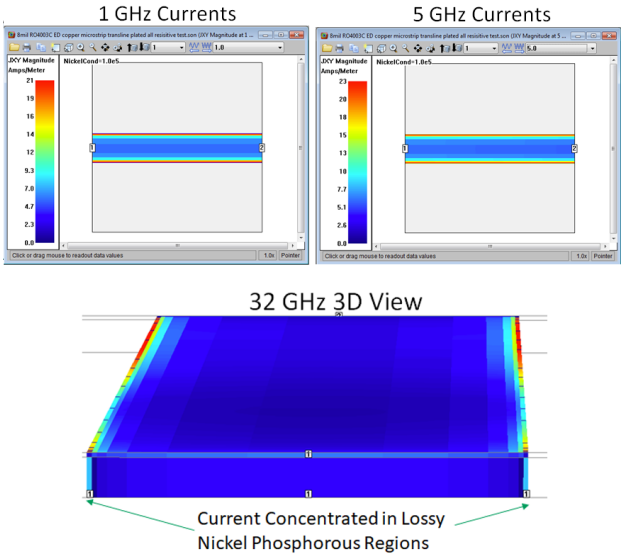

Fig. 3. Simulated cross-sections from Sonnet at 1 GHz (top left), 5 GHz (top right) and 32 GHz (bottom). With increasing frequency, the current is increasingly in the sides of the conductor, where the more-lossy nickel-phosphorous resides.

metal. This is of course due to edge-effect "pushing" current towards the edges, and the effect increases with frequency as with skin depth. These observations illustrate the importance of the inclusion of side-profile nickel-phosphorous in the model.

C. Specific Model Parameters

Geometric parameters are inherently available for the general circuit geometry, and parameters for the metal plating are available from standard [6]. For this work, thickness of the

nickel layer is considered to 0.5 μm, and the gold layer is considered to be 0.08 μm. As the gold is extremely thin, it is omitted from this study. Surface roughness parameters for both RA and ED copper are often available and are included in this model, the importance of which is thoroughly demonstrated in [4]. Further, the copper conductivity is well known. It might be assumed that nickel conductivity is also well known, however, for corrosion protection, most ENIG processes plate with a nickel-phosphorous alloy as opposed to pure nickel. It is generally accepted that increasing phosphorous content will decrease conductivity, however, at the time of this writing precise conductivity values are not widely available. Given the importance of edge effect as detailed previously, the authors consider the value of conductivity to be paramount to accurate data. As such, a range of conductivities are simulated across a likely range (from 10^5 to 10^6 S/m) and overlain with measured data. While all simulations in this range are reasonably close (indeed, at low frequency there is very little difference between them), the conductivity value of the best matching data, 5×10^5 S/m, is considered to be the extracted value. Notably, tuning simulation parameters to match measured data is a procedure which requires great care, and thus the extracted value is used in two other topologies for separate verification.

IV. Measured and Calculated Data and Analysis

This section compares measured data and simulated data across the three main test topologies.

A. RT/duroid® 6002 laminate microstrip RA

The first test case is the most optimized for detection of ENIG plating effects on IL. It features the thinnest substrate at 0.005" (0.127 mm), the lowest loss substrate minimizes the effects of dielectric loss, and the RA metal minimizes the effects of surface roughness. As such, the results are shown in the top left of Fig. 4. Good agreement is observed, with maximum error of approximately 0.07 dB/in. for bare copper and 0.12 dB/in. for plated, with the average error significantly lower. Notably, the bare copper data and ENIG data sharply diverge between approximately 3 GHz and 10 GHz, where the skin depth is approaching and exceeded by the thickness of the nickel-phosphorous.

B. RO4003C™ laminate microstrip ED

A more common configuration, the thicker 0.008" (0.203 mm) substrate and ED metal present a different topology with which to test the efficacy of the model. Results are shown in the top right of Fig. 4. Again, agreement is observed with a maximum difference of approximately 0.09 dB/in. for bare copper and an average of 0.13 dB/in. after ENIG application. A similar divergence is viewed with respect to frequency. This is the second topology for which the extracted value of conductivity for the nickel-phosphorous has proven effective.

C. RO4003C™ laminate GCPW ED

It is of interest to test a third circuit with an entirely different topology featuring significantly different field distributions.

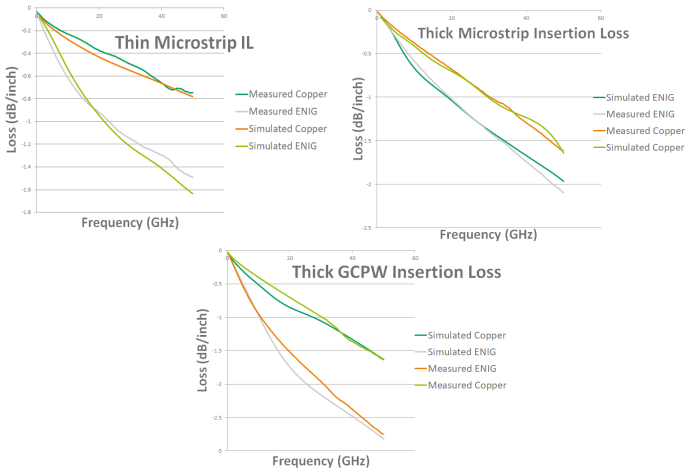

Fig. 4. Simulated vs measured data for the thin microstrip test (top left), thick microstrip test (top right) and thick GCPW test (bottom). Agreement is reasonable and the frequency behavior of the ENIG plating suggests strong dependence on edge-effect.

As such, an GCPW test is run on a similar substrate to the previous section. The bottom of Fig. 4 shows results. Maximum error observed for bare copper is approximately 0.17 dB/in. and for ENIG, 0.25 dB/in., and again, average error is significantly less. This adds further credence both to the model as well as to the extracted conductivity value.

V. Conclusion

A number of circuits and topologies have been designed, built, simulated, and measured, in an effort to produce an efficient, high-frequency model that can predict the effects of the commonly-applied ENIG finish. Reasonable agreement is observed across all topologies over an extremely broad band from 1 to 50 GHz. Further, the contributions of side-profile plating, nickel-phosphorous characterization, and measurements to 50 GHz are made. This suggests that the detailed method of modeling ENIG plating with a self-extracted conductivity may be viable for accurate simulation of such circuits at the higher frequencies used by 5G circuits.

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