

Free EM Simulator Analyzes Spiral Inductor on Silicon

by

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Abstract

A spiral inductor on silicon is investigated in detail using the free Sonnet Lite 3-D planar electromagnetic analysis. First, a baseline inductor is evaluated and the Sonnet Lite model is simplified for the fastest possible analysis while maintaining accuracy. Then various parameters of the inductor are modified in order to determine how they affect loss. Modified parameters include the dielectric constant and thickness of a thin insulating dielectric layer, line width and spacing. Quantitative evaluation of analysis error bounds is also provided.

Introduction

Spiral inductors have a deceptively simple geometry but are notoriously difficult to analyze. Add the complexity of a conductive silicon substrate and the problem pushes the limits of even the most advanced analysis capabilities available today. In this paper, we demonstrate how Sonnet Lite can be used to provide a high accuracy solution to this problem.

Sonnet Lite is an electromagnetic analysis of 3-D planar circuits based on the industry standard Sonnet Suite. It is available for free download from <http://www.sonnetusa.com> (about 14 Mbytes) or on CD-ROM from Sonnet Software (315-453-3096) for the cost of shipping. Sonnet Lite is not a demo, it is real software. Sonnet Lite can handle all small to medium size problems using up to 16 Mbytes of RAM (full matrix solve), up to two metal levels (three dielectric layers), and up to four ports. With care, a large number of problems can be solved within these constraints. The spiral inductor on silicon is one such problem.

The basic characteristic of Sonnet that makes it ideal for this problem is the accuracy with which conducting dielectrics are analyzed. Sonnet is an FFT (Fast Fourier Transform) based analysis. As such, there is no accuracy degrading numerical integration. In addition, all fields in each layer are represented as a (large) sum of simple rectangular waveguide modes (the side walls of the conducting box containing the circuit form the rectangular waveguide). When loss is present,

we need only change the characteristic impedance and velocity of propagation of each waveguide mode. Since these characteristics are known exactly for rectangular waveguide, substrate conductivity is included with precisely the same accuracy as is seen in an equivalent lossless analysis. This is difficult to do in analyses based upon direct numerical integration of an underlying Green's function.

Thus, the only problem to be overcome in analyzing an inductor on silicon using Sonnet Lite is to cast the problem into a form that satisfies the analysis constraints.

Base Line Inductor

Figure 1 shows the base line inductor. To reduce substrate loss, we are using a coplanar inductor. The coplanar ground strips are the wide conductors in Figure 1. Ground return current flows in these strips. Thus, the electric field from the signal line to ground need not pass through the entire silicon substrate. This results in lower loss.

The inductor's transmission lines are 8 microns wide with 8-micron separation. The ground strips are 16 microns from the edge of the inductor. The substrate is 1000 microns thick with a relative dielectric constant of 12.0 and a conductivity of 20.0 S/m. In addition, there is a 1-micron layer of SiO₂ with a relative dielectric constant of 4.0 on top of the silicon. Most of the inductor is on top of the SiO₂ layer. The connection from the center of the inductor out is below the SiO₂ on top of the silicon. Metal loss of 0.04 Ohms/square (plus appropriate skin effect) is included.

Our first task is to simplify our model of the inductor without significantly affecting accuracy. Sonnet meshes only the metal surface and problem size increases rapidly with the number of subsections. Thus, we want to reduce the number of subsections as much as possible.

The first way we can do this is by making the subsection size as large as possible. With 8-micron wide lines on 16-micron centers, that is easy. We simply choose an 8-micron cell size. Now all 8 micron lines are meshed one cell wide. This does impact analysis error, but this is something we shall quantitatively evaluate later.

The other way we can reduce the subsection count is by reducing metal area. The coplanar ground return lines are wide. It would be nice to eliminate them from the analysis. This is easily done when we realize that Sonnet Lite places a perfectly conducting box sidewall at the edge of the substrate. Let's remove each ground strip and substitute a box sidewall in its place. Now the ground current flows in the box sidewalls rather than in the ground strips. Let's try placing the sidewalls 24 microns from the inductor (the ground strips were 16 microns away), see Figure 2.

This is a major modification to the circuit and one would do well to wonder if it might fail. As an alternative to pointless hand waving, electromagnetics allows us to arrive at a firm quantitative answer. Figure 3 shows a comparison of the two approaches to this analysis. S₁₁ is different by about 0.5 dB. S₂₁ differences approach 2 dB, but only at high frequencies where S₂₁ is down about 20 dB. We shall assume that these differences are small compared to requirements

and proceed with the evaluation of the inductor of Figure 2. On a 450 MHz Pentium the inductor of Figure 2 analyzes in 1 second per frequency and uses only 1 Mbyte of RAM. The original inductor requires 2 Mbytes and 2 seconds per frequency. While this is a small difference now, it becomes important later. This is why we shall continue with the inductor of Figure 2.

If the half-dB difference is significant, we can perform our tradeoffs as below using the Figure 2 inductor. When complete, we can then perform one final analysis with all of our changes incorporated into the Figure 1 inductor if desired.

Error Bounds

At this point it is appropriate to determine the accuracy of the analysis. While all electromagnetic analyses are advertised as being very accurate, as engineers we are more interested in analysis error than we are in analysis accuracy. Furthermore, we would like to have a quantitative value for the error. By comparing the estimated error with our project requirements, we can tell whether or not the trust we place in our analysis is justified.

The error mechanisms for Sonnet have been extensively investigated. In nearly all cases, the principal error source is error due to cell size. In addition, this error has the unique characteristic of reducing by half when cell size is cut in half (with a few well-understood exceptions).

Error due to cell size is easily evaluated. If we cut the cell size in half and analyze the circuit, then we also cut the error in half. If we know half the error, we can easily calculate the total error.

The results of just such a convergence analysis are shown in Figure 4. The original cell size is 8 microns. The second analysis uses a 4-micron cell size with an analysis time of 6 seconds per frequency. The difference between the two curves is not easily seen, but is less than 0.15 dB nearly everywhere. This means that results obtained using the 8-micron cell size should be good to about +/- 0.3 dB.

If this is sufficient for your needs, we can just stop here. However, if you need more accurate results, we can do what is known as a "Richardson extrapolation". Determine the total error for each data point as above (i.e., double the difference between the 8 and 4 micron cell size results), and then subtract the error from the 8 micron answer. A spreadsheet is useful for performing a Richardson extrapolation. Results should now be accurate to about +/- 0.05 dB or so. Not bad for free software!

To have maximum confidence that a Richardson extrapolation is working, one should also perform a third analysis at 1/4 cell size. We did so with the full Sonnet Suite (the problem is just a little bit too big for Sonnet Lite) and confirmed that the result is converging as expected.

As you may have noted, there is one exception to the +/- 0.3-dB error bounds. The lowest frequency S_{21} data point, 100 MHz, appears to be incorrect. This can happen in any

electromagnetic analysis when cell size is very small compared to wavelength. The 200 MHz point is much better but still seems to have a bit of error. Above 200 MHz there is no problem.

We are including the low frequency data to demonstrate that no electromagnetic analysis can be trusted completely. One should always perform some kind of convergence test and view the results with a critical eye to error, as we have done here. This approach eliminates surprises later.

The Lossless Limit

Before we start trying to reduce loss, let's perform an analysis with loss completely removed. Comparing a lossless analysis with the baseline lossy analysis gives us an upper limit on how much we can possibly improve the inductor. We removed all loss (metal and substrate) from the inductor of Figure 2 and analyzed the resulting circuit. In Figure 5, we compare the lossless analysis with the original lossy result.

There is around 7 dB of loss in both S_{21} and S_{11} at 40 GHz. There is a lot of room for improvement, if only we can figure out how to do it. By comparing S-parameter data for the lossless case, the baseline case, and each case we wish to consider, we can quickly determine the merits of each alternative. Note that there is no need to calculate inductor Q, which, for the complicated equivalent circuits possible with planar spiral inductors, is not uniquely defined nor simple to calculate.

Line Width

Next, taking the baseline inductor of Figure 2, we increase the line width. The reasoning here is that a wider line width should yield lower loss. We increased the line width from 8 microns to 12 microns (4 micron cell size), Figure 6. The analysis result is shown in Figure 7. The analysis now requires 11 seconds per frequency. Note that the loss has generally increased. While the effect of conductor loss has undoubtedly gone down, the effect of substrate conductivity has increased.

The loss drops unexpectedly around 40 GHz. The reason for this has not been investigated. It might be due to a resonance off the plot above 40 GHz.

If wide lines don't work, let's try narrow lines. Figure 8 shows line width decreased to 4 microns and Figure 9 shows the analysis results (5 seconds per frequency). Loss has gone down substantially. If desired, we could continue until we find the optimum line width.

Insulating Layer Thickness and Dielectric Constant

A spiral inductor on silicon usually has a thin insulating layer (for example, SiO_2) deposited underneath it. This reduces the effect of substrate conductivity, especially at low frequency. To

reduce the loss, one might try making the insulating layer thicker or choosing a material with a lower dielectric constant.

To investigate these alternatives, we first increase the insulating layer thickness from 1 micron to 2 microns. The result is shown in Figure 10. Next, using the original 1-micron layer thickness, we change the dielectric constant from 4.0 to 2.0. The result is in Figure 11. Both actions substantially reduce inductor loss at all frequencies.

Now, with knowledge of the relative importance of each parameter with respect to loss, and with knowledge of manufacturing and design constraints, the designer can choose a design to realize the lowest possible loss.

To gain some further insight into this particular spiral inductor design, we analyzed the spiral inductor of Figure 2 with extremely small cell size, 0.5 micron. Due to the size of the problem, we used the full Sonnet Suite. Thus, each line is 16 cells wide. The resulting current distribution is shown in Figure 12. Note that there is some disruption of the current distribution at the location of the underpass connection to port 2. This is common in underpass and overpass situations and is real. It is not a numerical artifact.

In Figure 12, red represents about 1200 A/m. Port 1 is excited with a one-volt source at 40 GHz connected in series with a 50-Ohm resistor. Port 2 is terminated in 50 Ohms. The analysis requires over 12,000 subsections and 305 Mbytes of RAM. Because the computer has only 256 Mbytes of RAM, substantial swapping increased analysis time to about 8 hours. Normally, we would expect about one hour.

Conclusion

We have demonstrated how the free electromagnetic software Sonnet Lite can be used to solve what was once a difficult and troublesome problem, a spiral inductor on a conductive silicon substrate. In addition, we have shown how to modify the inductor so as to reduce inductor loss and how to characterize the analysis error quantitatively. We have also described how to use the well-established "Richardson extrapolation" to substantially reduce error even further without resorting to the full Sonnet Suite. With the approaches described here, we expect that Sonnet Lite can solve all but the most difficult of 3-D planar EM problems.

Acknowledgement

Sonnet Lite was made possible because of work funded by DARPA under the MAFET program.

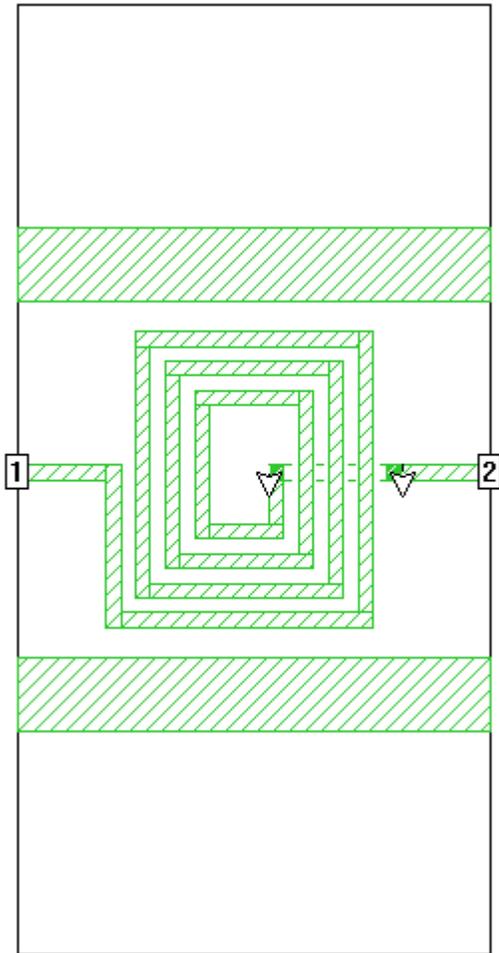


Figure 1. The base line inductor includes coplanar ground return lines for low loss.

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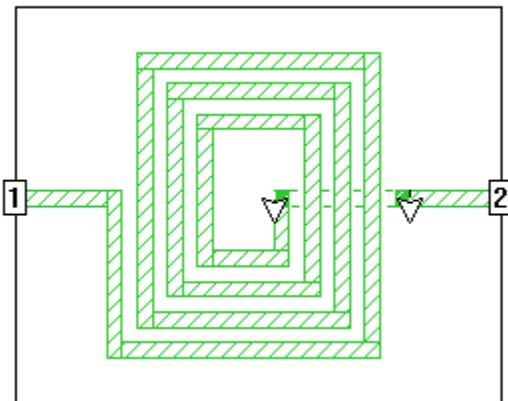


Figure 2. The inductor of Figure 1 modified so that the box sidewalls take the ground return current. Removing the ground strips results in a faster analysis.

File: sbase.tif

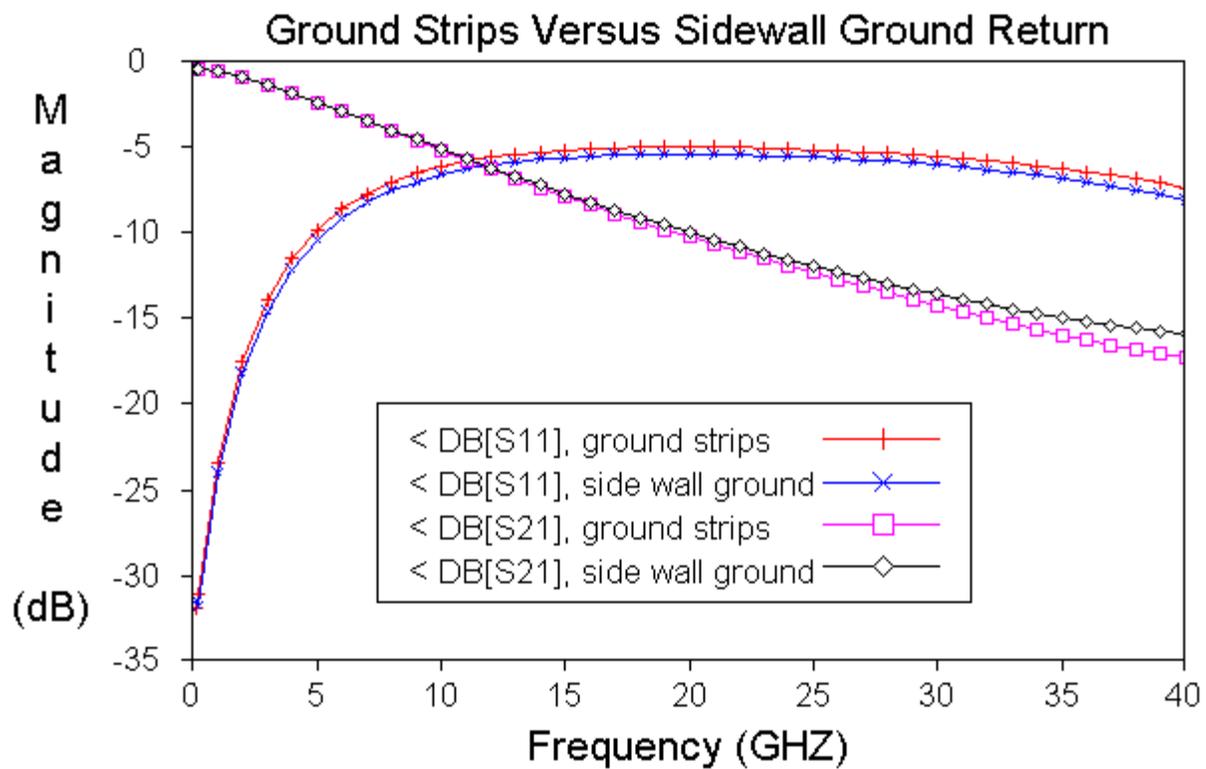


Figure 3. Comparison of analysis results from the inductor of Figure 1 with the inductor of Figure 2. S_{11} differences are about 0.5 dB. S_{21} differences approach 2.0 dB, but only at high frequency.

File: Figure3.tif

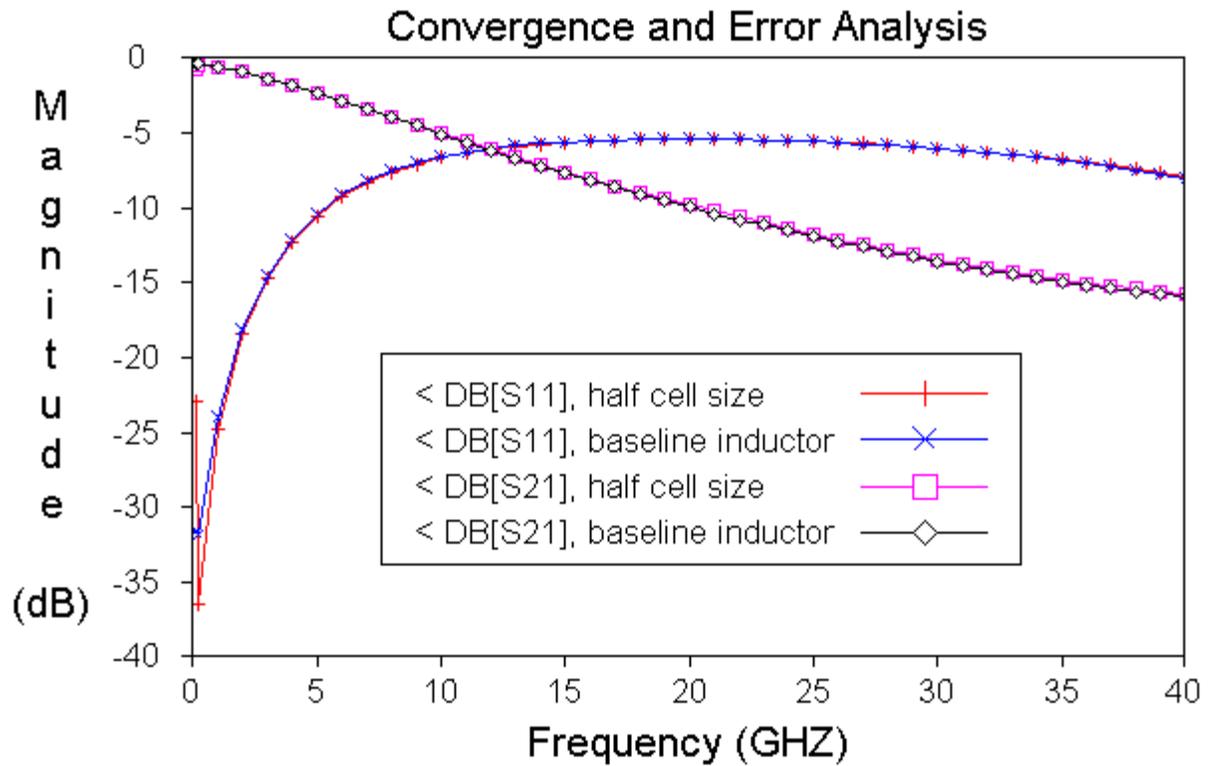


Figure 4. By cutting cell size in half (from 8 to 4 microns) we can determine error bounds for the analysis results. With at most 0.15 dB difference between the two results, we can be reasonably confident that the 8 micron cell size result is within +/- 0.3 dB of the correct answer.

File: Figure4.tif

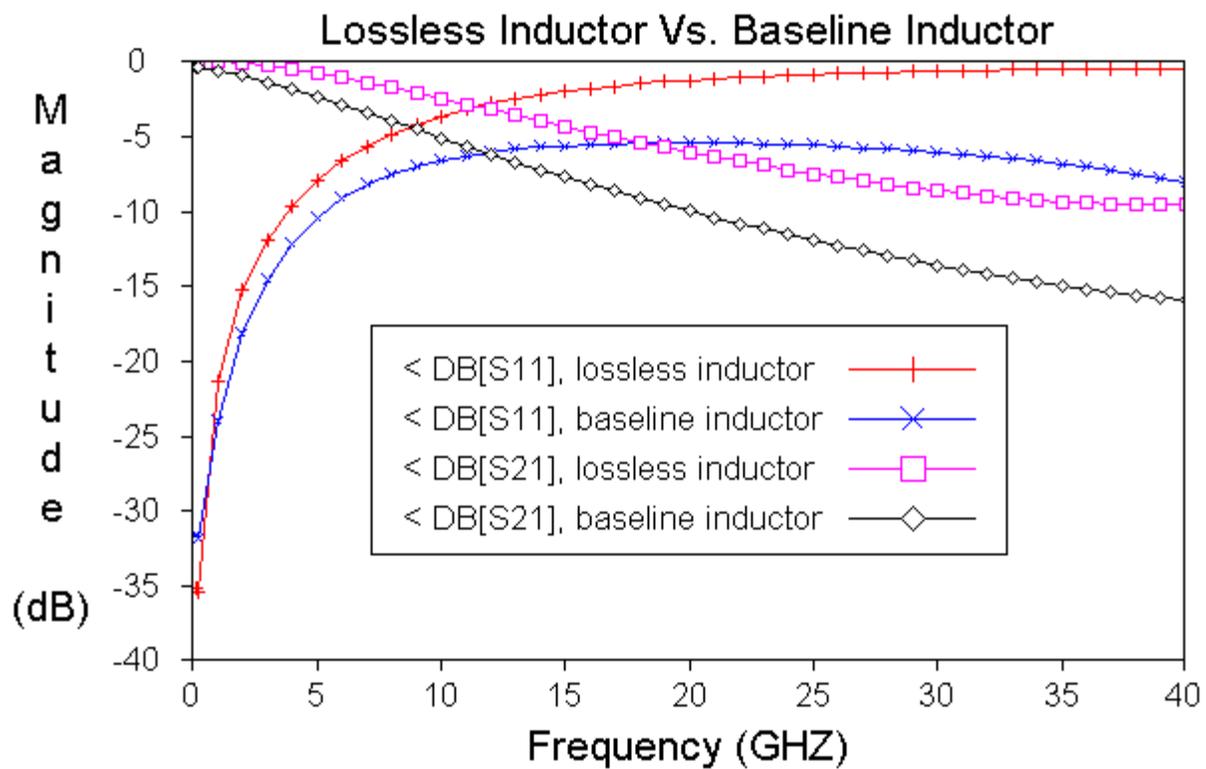


Figure 5. Comparing the baseline inductor (from Figure 2) with the same inductor with all loss removed shows that we have room for about 7 dB of improvement at 40 GHz.

File: Figure5.tif

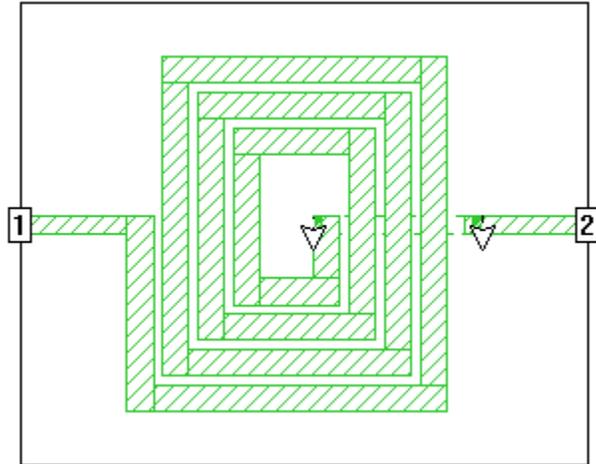


Figure 6. The line width is increased from 8 to 12 microns to see the effect on loss.

File: Width12.tif

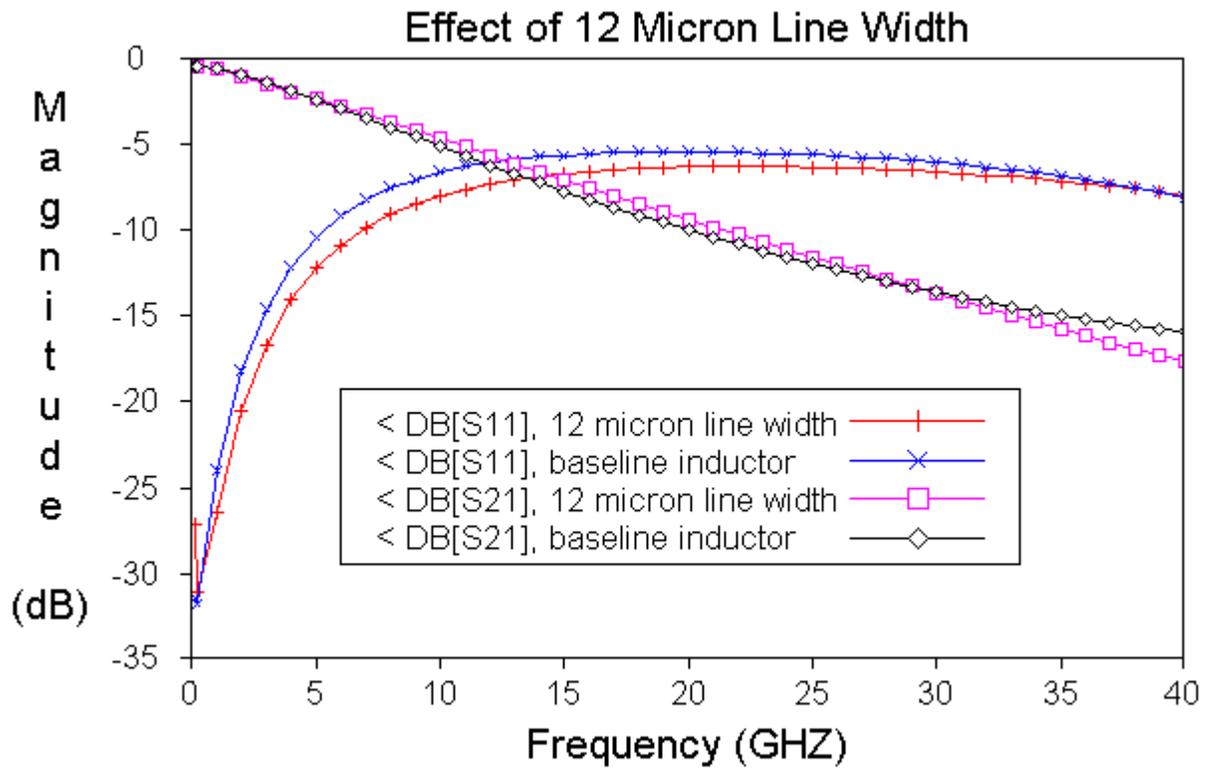


Figure 7. Increasing the line width from 8 to 12 microns unexpectedly increased loss.

File: Width12_plot.tif

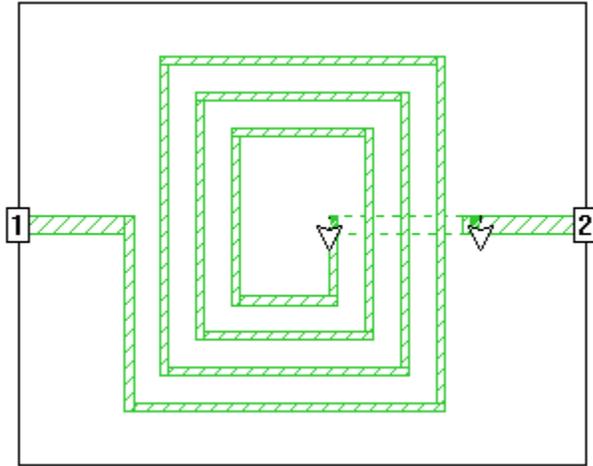


Figure 8. Decreasing the line width from 8 to 4 microns results in this geometry.

File: Width4.tif

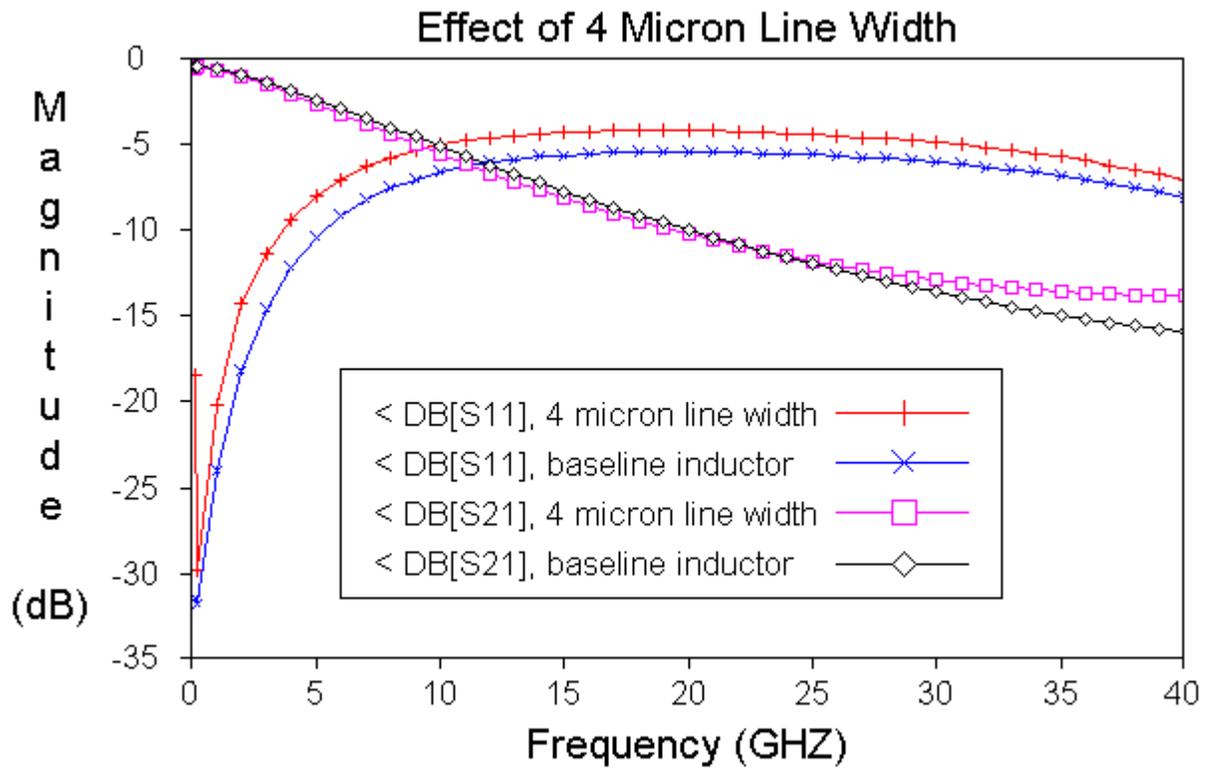


Figure 9. Decreasing line width from 8 to 4 microns results in the desired decrease in loss.

File: Width4_plot.tif

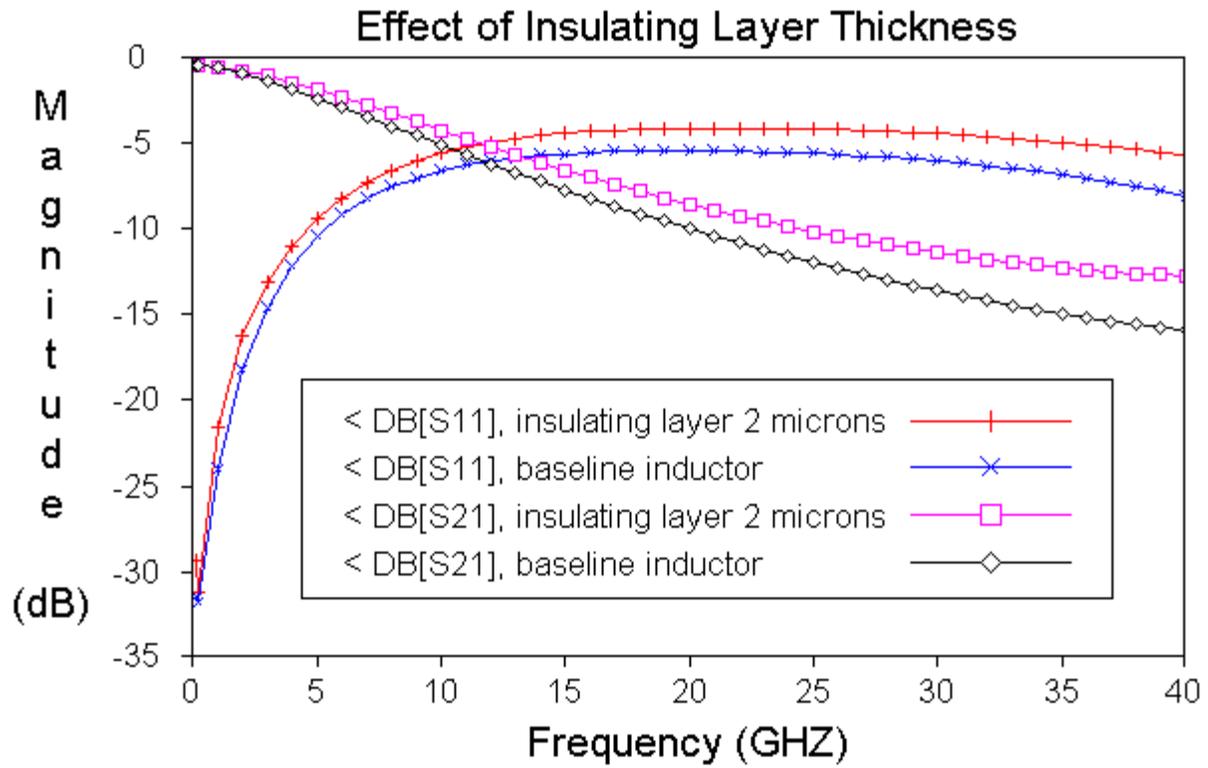


Figure 10. By increasing the thickness of the insulating layer on top of the silicon substrate from 1 to 2 microns, we reduce the inductor loss substantially.

File: Thicker.tif

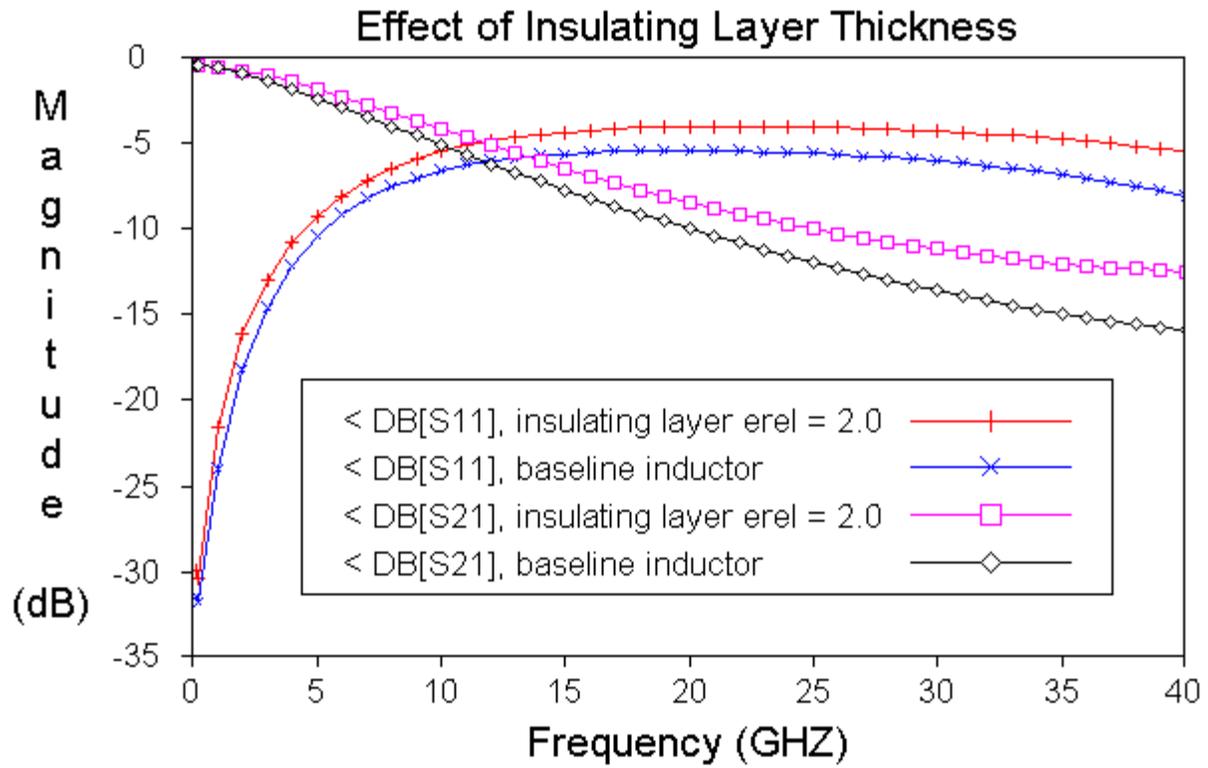


Figure 11. By decreasing the dielectric constant of the thin insulating substrate on top of the silicon substrate from 4.0 to 2.0, we likewise reduce the inductor loss substantially.

File: Erel2.tif

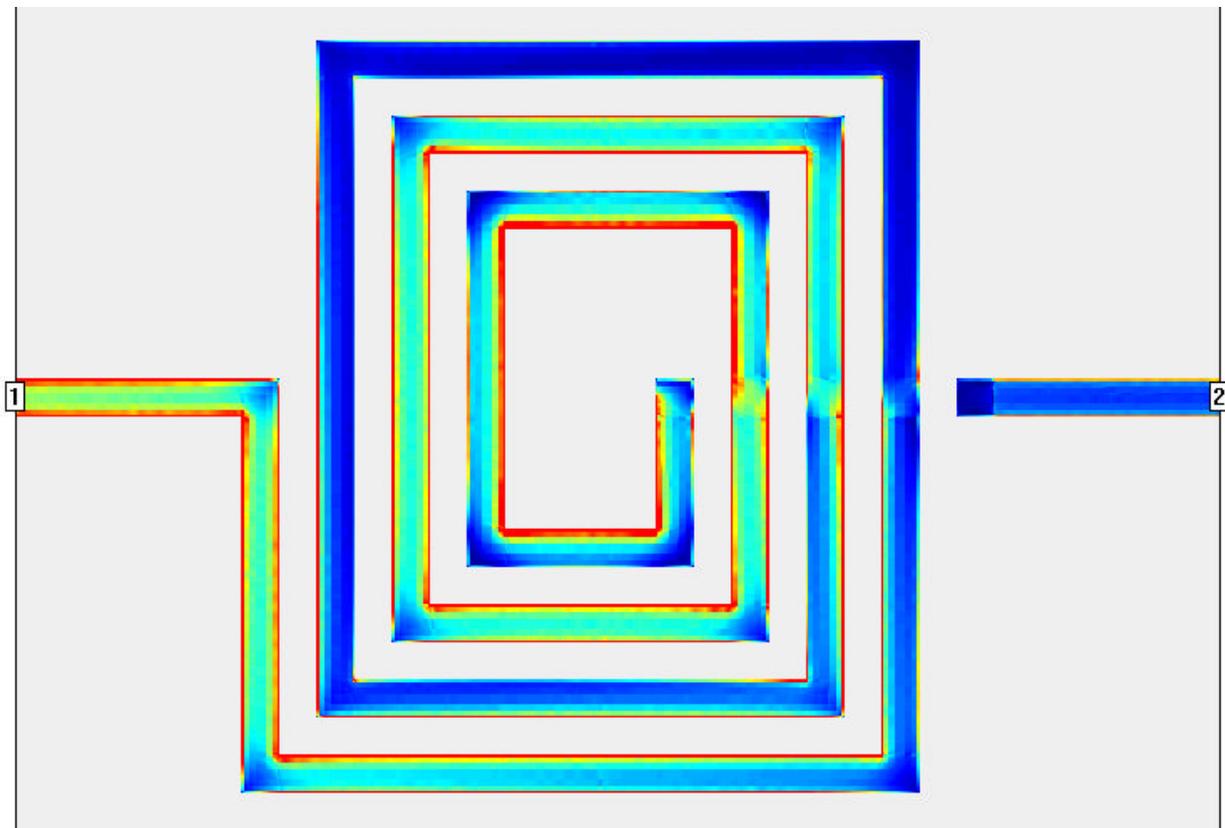


Figure 12. The current distribution for the baseline spiral inductor analyzed with a very fine 0.5 micron cell size. The disruption near the underpass connection to port 2 is real, it is not a numerical artifact.