

Simulation and Layout of On-Chip Microstrip Patch Antenna in Standard CMOS Technology

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Abstract: This paper provides the steps needed to design and simulate on-chip millimeter-wave Microstrip Patch Antenna using the electromagnetic field solver Sonnet to achieve the required matching impedance and hence the desired oscillation frequency. In addition, key layout issues are discussed for the $0.18\mu\text{m}$ standard CMOS technology. The system designed and tested consists of a lateral IMPATT diode and on-chip antenna. Sonnet optimized the antenna's area to 1.4mm^2 at oscillation frequency of 77GHz . The measured transmitted power of the system had an offset frequency of -0.13% from the simulation results.

Keywords: Microstrip patch antenna, CMOS, Millimeter-wave, IMPATT diode, 77GHz

1. Introduction

The real challenge in designing millimeter-wave integrated transmitters is the matching of the active device to the antenna [1]. It requires careful optimization of the active device structure geometry and antenna layout based on the given parameters in the fabrication process [2]. In this work, the antenna impedance seen by the IMPACT Avalanche Transit Time (IMPATT) diode was simulated by the EM field solver Sonnet including key layout issues to achieve an error within less than 1% between the measured and the simulated oscillation frequency [3]

2. Design

The fundamental equation governing the oscillator design is the 'oscillator equation'. It must hold for all oscillators in steady-state operation (Fig.1). It states that the sum of the circuit impedance and the device impedance must be zero at the device's operating point [4].

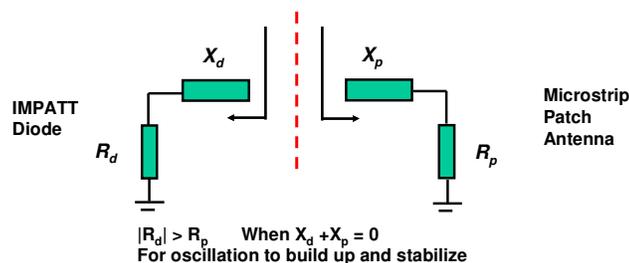


Fig. 1. Oscillator block diagram.

A. IMPATT Diodes Integrated in Coplanar Waveguides

These diodes have been monolithically integrated in coplanar waveguides and successfully characterized by S-parameter measurements from 40MHz to 110GHz (Fig. 2) [5]. By carefully

designing the Ground-Signal-Ground (GSG) pad we were able to mitigate the undesired oscillations that typically disturb S-parameter measurements of IMPATT diodes. The ground pad is 100µm x 100µm while the signal pad is 80µm x 80µm.

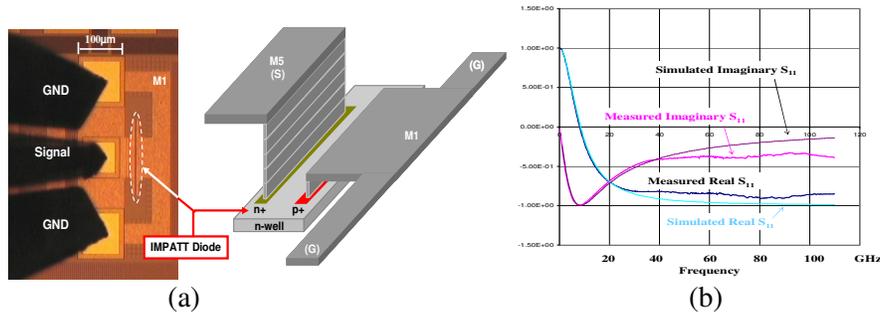


Fig. 2 (a) Die photo of the integrated IMPATT diode and the RF probe. (b) Comparison between the measured and the simulated S₁₁ for the GSG structure.

We used the electromagnetic field solver Sonnet to simulate the GSG structure and compared its S₁₁ to the measured one as shown in Fig. 2(b). A substantial difference is noticed after 40GHz which required some kind of correction while de-embedding the IMPATT impedance. The equivalent IMPATT impedance at 77GHz is shown in Fig. 3 for V_{bias} = 11v I_{diode} = 55mA, where R_d is the negative resistance associated with the reactive part which is capacitive.

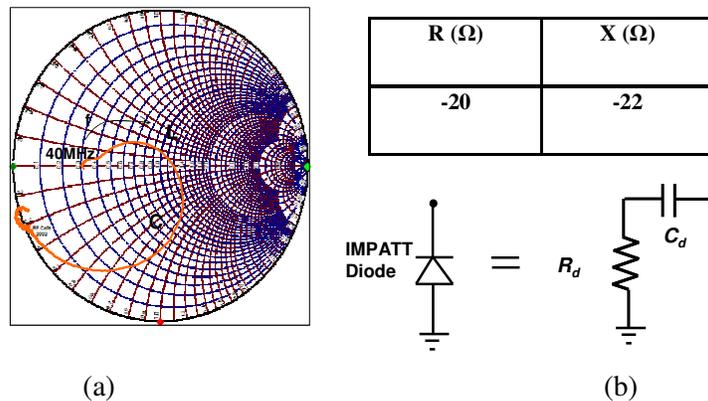


Fig 3 (a) Measured reflection coefficient of a CMOS IMPATT diode at maximum frequency of 110GHz prior to de-embedding. (b)Equivalent IMPATT impedance model at 77GHz for V_{bias} = 11v I_{diode} = 55mA.

B. Microstrip Patch Antenna

Measurements and simulations reveal that the CMOS IMPATTs are capable of generating high negative resistance and sustaining oscillation at 77GHz, provided that the resonator resistance is below 20Ω, and the reactive parts of the antenna and the diode impedances cancel [3]. The diode’s depletion region capacitance introduces a loading effect, so that the length of the patch antenna is reduced relative to that of an equivalent standalone resonator operating at the same frequency. By examining various Layout structures, and taking into consideration the factors summarized in Fig. 4 and provided for the technology used, a 750µm x 1850µm microstrip patch antenna (Fig. 4) was found to match the impedance requirements of the IMPATT diode best. The calculated input impedance of the microstrip patch antenna seen by the IMPATT diode versus frequency is depicted in Fig. 5. Since matching is obtained when Z_{diode} + Z_{antenna} = 0, the intersection between the negative reactance of the IMPATT diode and of the microstrip patch antenna determines the oscillation frequency.

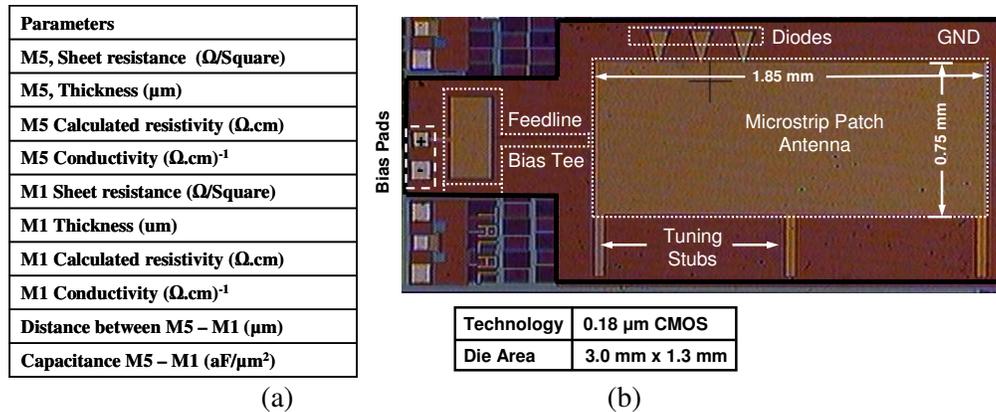


Fig. 4. (a) The parameters needed to perform the Patch Antenna simulations at 0.18 μm CMOS Technology. (b) Die photo of monolithic IMPATT transmitter in standard CMOS technology.

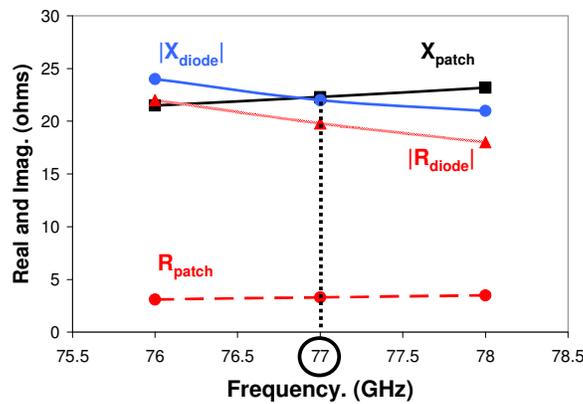


Fig. 5. The real and imaginary parts of the IMPATT diode and the antenna.

The simulated directive gain is 11dB as shown in Fig. 6 with a 4 μm dielectric thickness for the patch antenna. This clearly shows the necessity of some form of beam shaping for practical applications. More simulated results are summarized in Fig. 6 for different dielectric thickness.

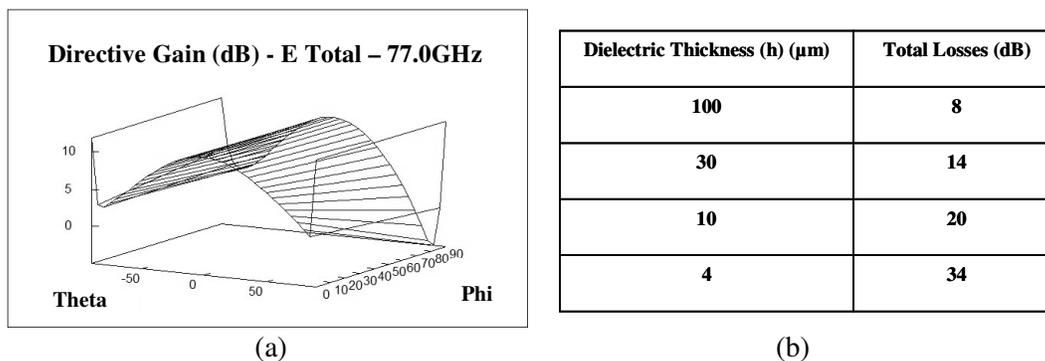


Fig. 6. (a) The simulated directive gain of the CMOS microstrip patch antenna. (b) Simulated Antenna loss by Sonnet for various dielectric thicknesses.

Simulations of antenna performance comprehend multiple factors, such as; feed type, transition and location, antenna stubs, via parasitics, dielectric cover (passivation layer), finite ground plane, as well as the substrate doping profile of the CMOS technology used [6].

B.1 Feed Type, Transition and Location

The tapered feed, with a 150 μm length, provides the best matching range with respect to the measured IMPATT impedance as shown in Fig. 7.

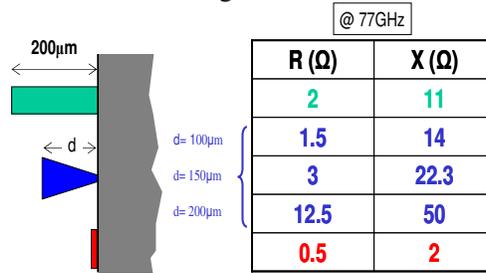


Fig. 7. The feed type and the associated input impedance of the antenna using each type.

Feed transition acts like inductive reactance and provides smooth transition between the IMPATT diode and the antenna, hence reducing the reflected wave (Fig. 8). The probe with a 150 μm length with a 100 μm was the best choice especially with the diode width which is also 100 μm .

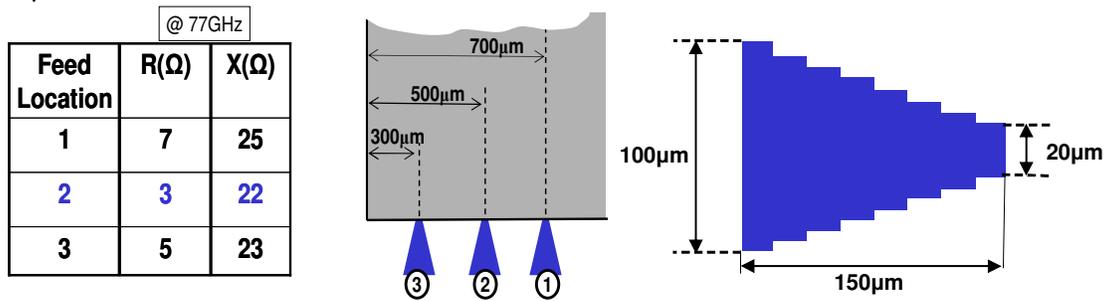


Fig. 8. The feed point location, the feed type and the feed transition from the IMPATT diode to the patch antenna.

As shown in Fig. 8, the feed location has a greater influence on the real part of the antenna impedance compared to the reactive one. We used the three locations in the final layout to increase the probability of matching between the IMPATT diode and the antenna.

B.2 Antenna Stubs

Furthermore, three stubs are added to the antenna (Fig. 9). The stubs connect to one of the radiating edges of the antenna to provide a means for some post-fabrication tuning. We simulated different stub dimensions; for example, three 50 μm x 200 μm stubs could provide a tuning range for the real and the imaginary part of 8% and 2%, respectively. If we increase the length to 300 μm to have three 50 μm x 300 μm stubs, then the real and the imaginary parts of the antenna input impedance can be adjusted over a range of 20% and 3%, respectively. We chose the later for our final layout for the wider tuning range provided.

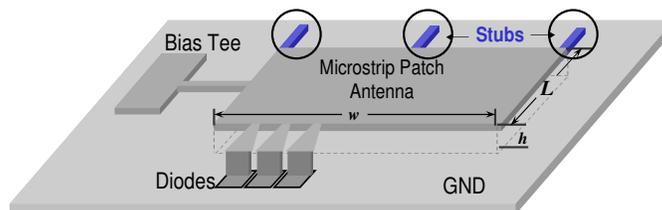


Fig. 9. The tuning stubs at one of the radiating edges.

B.3 Simplified Transmitter Model

The parasitics introduced by the vias and the metal layers (five layer in this process) connecting the IMPATT diode to the antenna were modeled using Sonnet as shown in Fig. 10 and summarized in Table 1. After inserting Z_1 , Z_2 , and C_{tot} , the simulation results reveal a degradation of the IMPATT real and imaginary parts by 25% and 5% respectively.

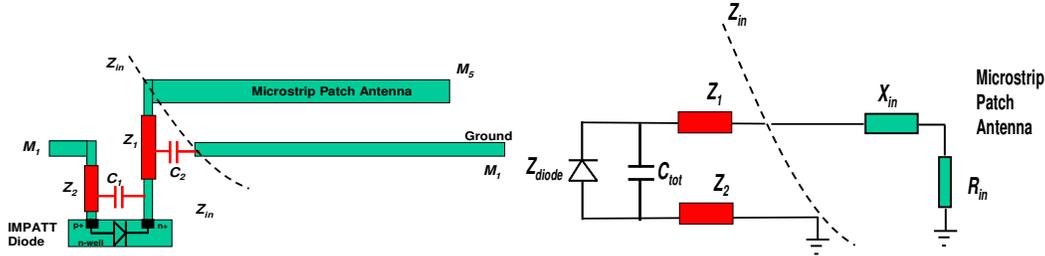


Fig.10. The antenna, the diode and all the equivalent parasitics included in the system.

Table 1: Summary of the simulated parasitics.

Component	Simulation results
Z_1	$0.5 + j 0.1 \Omega$
Z_2	$0.08 + j 0.02 \Omega$
C_1	11fF
C_2	0.4fF

B.4 Dielectric Cover

As the design rules prevent having large passivation opening (Fig. 11) to cover the antenna area, we had to study and simulate the effect of the dielectric cover on the antenna impedance (Fig. 11). We noticed, with a cover thickness of $3\mu\text{m}$, an increase in the real and the imaginary part by 10% and 4%, respectively compared to the case with no dielectric cover, which we had to account for when designing the matching impedances.

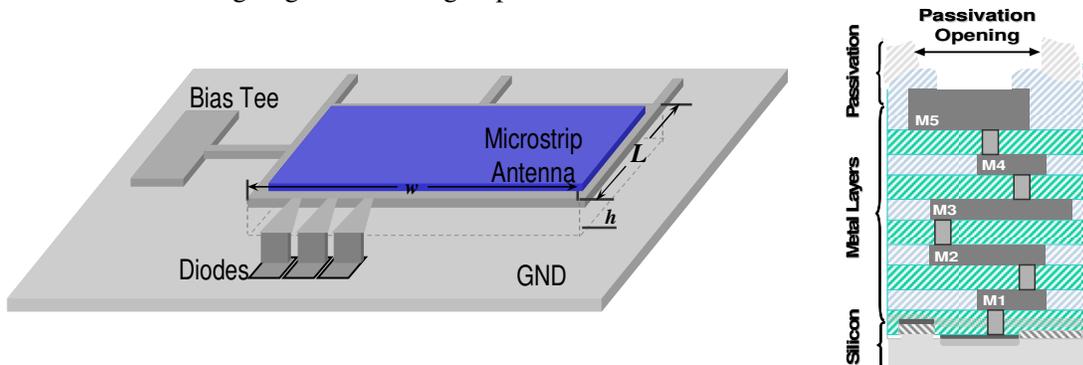


Fig. 11. The dielectric cover on top of the fifth metal layer on $0.18\mu\text{m}$ CMOS technology.

B.5 Effect of Finite Ground Plane

Even though it is a common practice to extend the ground plane to about six times the substrate thickness [4] to achieve results similar to that of the infinite ground plane, we decided to extend it even more to be 10 times, instead (Fig. 12). This provides more isolation for the antenna and prevent undesired coupling to the dummy structures scattered around the antenna. These dummy structures exist because of the design rules imposed on the layout [7].

3. Measurements and Results

To provide multiple designs, three identical diodes ($100\mu\text{m} \times 0.5\mu\text{m}$) are placed in the layout, each feeding the antenna at different locations (Fig. 13). Diodes can be tested individually by isolating the desired one using a YAG laser. This provides means of finding the best matching location, post-fabrication.

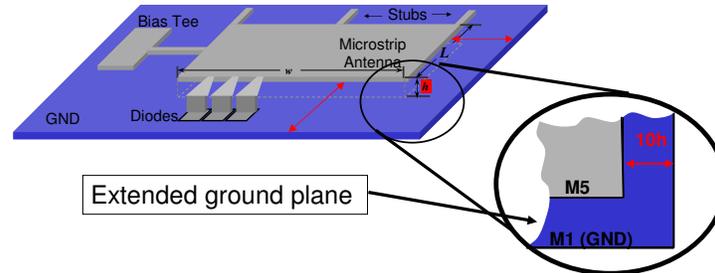


Fig. 12. The extension of the ground plane by 10h.

Among all the variations introduced in the layout to provide different designs, the one with the diode near the center of the antenna with all the tuning stubs, was the only working transmitter. When the on-chip transmitter is biased at 11V, the corresponding quiescent current is 30mA, and a signal is detected at an oscillation frequency of 76GHz.

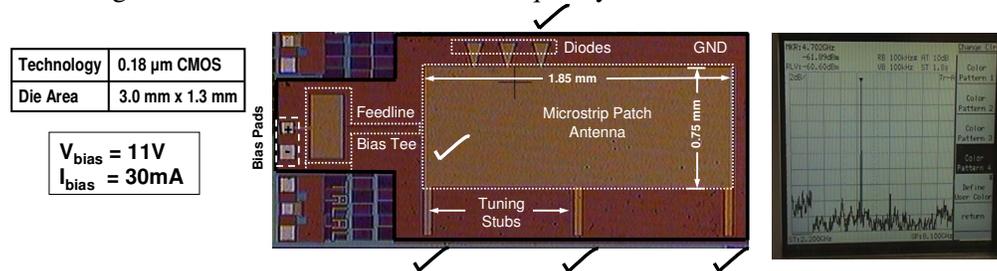


Fig. 13. The functional transmitter with the detected signal at 76GHz.

4. Conclusions

By using the EM field solver Sonnet, an on-chip Microstrip patch antenna was designed, simulated, and optimized at 77GHz. All key layout issues were included to accurately match the IMPATT impedance with the antenna.

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