Design of A Low Power CMOS Differential Low Noise Amplifier by Using Die-Level EM analysis

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Abstract: The performance of fully integrated CMOS Low Noise Amplifiers relies on the quality of the passive components available in the silicon process. The model accuracy of these passive components, especially the inductors, highly depends on their placement on the layout. Their performance often degrades due to the interactions of electric and magnetic fields between the nearby components. In order to model the on-chip passive components accurately die level electromagnetic analysis is often required in modern compact designs. It is not only helpful to predict the behavior of individual components but also useful to account for any coupling between them. As a result die-level EM analysis shortens the time spent in the lab to tune the circuit. This paper presents circuit simulation, electromagnetic analysis and measurement results of a low noise amplifier designed for Medical Implant Communication System.

Keywords: MICS, RFIC, Die-Level EM analysis, Differential CMOS LNA, Sonnet.

1. Introduction

The design of a Radio Frequency Integrated Circuit such as a fully integrated CMOS LNA requires tuning of intrinsic capacitances of transistors or parasitic capacitances associated with metal wires, pads and so forth. This tuning is needed to enhance the bandwidth of the circuit and is achieved by adjusting the values of passive components such as inductors, capacitors and resistors. The availability of inductors is one of the major differences between a standard CMOS and an RF CMOS processes. The inductors are scalable in most of the RF CMOS processes to help the designer chose from the list without requiring extra modeling activity. The designer specifies the parameters such as the outer diameter, r, the metal width, w, the underpass width, uw, the spacing, s, and the number of turns, n, to obtain the desired inductance value, the quality factor, Q, and self-resonance frequency. The inductance value can then be estimated by [1]

$$L = \mu_0 n^2 r \tag{1}$$

A significant amount of publication exists for modeling, design, and implementation of spiral inductors. Figure 1 depicts a widely used inductor model [2] with intrinsic parasitic components. Rsi and Csi model the losses in silicon substrate, RS is the series resistance of the metal layer, LS represents the desired inductance and CS is the horizontal capacitance between the adjacent metal layers in the inductor winding. COX is the capacitance between the inductor and the substrate.

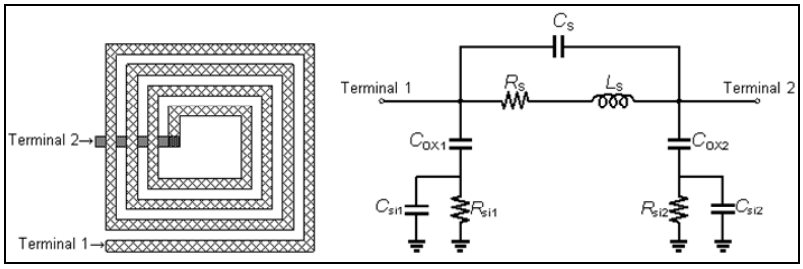

Fig. 1. *Planar spiral-inductor and its parasitic model*

The model based tools such as ASITIC [3] and Virtuoso Passive Component Designer are able to calculate the parameters of the inductor for a pre-determined layout view. Computer based modeling for any inductor with arbitrary layout requires a full-wave EM analysis. The EM solvers give more accurate results by considering secondary effects. The planar nature of CMOS process allows the planar EM simulators such as Sonnet [4] to give the faster EM solution of the structures. In particular, Sonnet has the Adaptive Band Synthesis technique which shortens simulation time without sacrificing the accuracy.

2. Design of a Differential LNA and Die-Level EM Analysis

The differential Low Noise Amplifier presented in this study is designed for Medical Implant Communication Systems [5]. Compactness of the circuits is extremely important for any implant applications. Figure 2 shows the schematic of the source-degenerated differential LNA topology. The major advantage of differential LNAs over single-ended ones is their much lower susceptibility to the common-mode noise injected through the substrate or the supply terminals. When a complete system is integrated on a single die, this issue becomes extremely important since the clocked digital circuits such as the ones in the baseband or the PLL are good sources of in-band noise and interference which degrade the performance. The second major advantage is their superior performance in alleviating the LO leakage problem. The differential LNA is biased in sub-threshold region to minimize its power consumption.

The drain inductors LD1 and LD2 are used to tune the LNA for its operation in the 402-405 MHz range. The inductors resonate with the capacitances at the drain nodes of M3 and M4 at the operating frequency. All of the inductors used in this circuit are planar spiral inductors with octagonal shape and they are implemented using the 6th metal layer which is the thickest metal layer of the process.

In order to account for every coupling mechanism during the design, a full-wave EM simulation is required on the entire die layout. Figure 3 shows the 3D view of the CMOS LNA in the EM simulator. The computing resources needed for such a simulation depends on the complexity of the CMOS process and the circuit layout. It is highly impractical for this CMOS LNA as it requires extremely large computing resources. There is extensive modeling activity involved in such simulations. Since the transistors are semiconductor devices, the conductivity of the channel in each transistor depends on its bias level. In order to simulate the transistor in an EM simulator, the sheet resistance (rho) for the channel and bulk layers for each transistor should be modeled in their respective bias point through the measurements. Then a special EM transitor model should be generated. Each transistor in the layout

should be replaced with the respective EM model where the channel is assigned its own EM layer with modeled substrate dielectric constant and conductivity. There are different techniques to model the channel resistor. The DC van der Pauw [6] is one of the widely used ones in the industry.

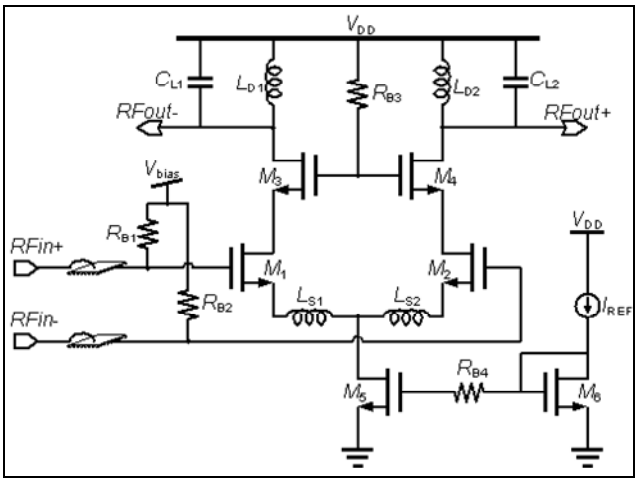

Fig2. Schematic of Differential LNA

The EM simulation for this design is done on the inductors and routing only. The LS1, LS2, LD1 and LD2 source and drain inductors shown in Figure 3 are simulated with exact process dielectric and metal stack-up by using the planar EM solver, Sonnet.

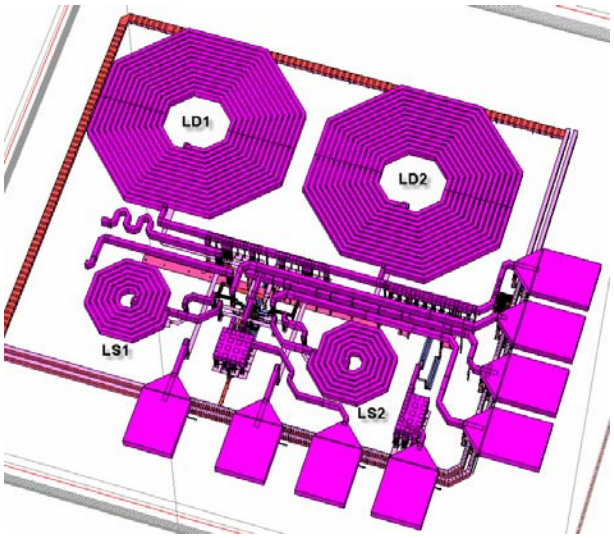

Fig. 3. The 3D view of the LNA layout in EM simulator

The EM simulated inductance and quality factor value for one of the drain inductors is shown in Figure 4. The effect of the proximity of inductors is seen clearly through the EM simulations.

The inductors LS1 and LS2 contribute to the real part of the input impedance at the gates of M1 and M2. They are part of the noise matching of the LNA. The initially they are selected from the model based inductor selection tool in the design kit. Each has the value of 2.78-nH. The quality factor is listed as 1.85 at 404 MHz. The self-resonance frequency is 16 GHz. The maximum Q factor value of 8.45 occurs at 7.15 GHz. The EM simulation shows that there is only small amount of raise in the source inductance due to the routing. The total EM simulated inductance value for LS1 is 2.98nH. The quality factor is

calculated to be 1.83 from the EM simulations.

The simulation testbench includes s-parameter files of the source and drain inductors obtained through the EM simulation. Thus the behavior of the circuit can be predicted more accurately by co-simulating schematic in spectre with Sonnet supplied EM solutions.

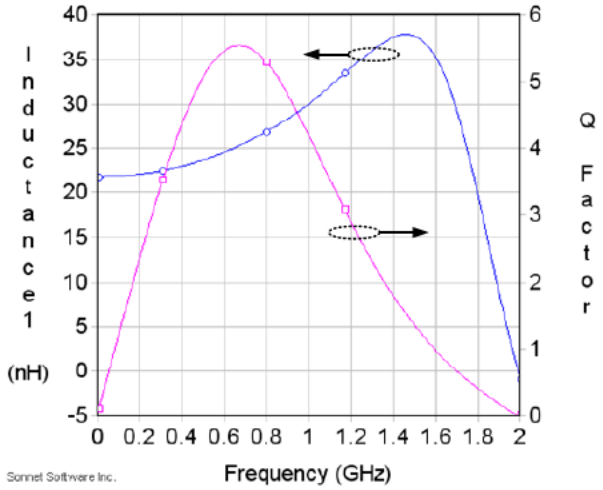

Fig. 4. EM simulated inductance and quality factor vs. frequency for L_{D1}

The source-pull technique is employed to match the complex input impedance of input transitors, M1 and M2, for optimum power and noise performance. The initial calculations were done based on the Power Constrained Simultaneous Noise and Input Matching technique [7]. However, the calculated transistor sizes were too large for practical implementation. Therefore, the device widths are optimized to 350-µm.

The total DC current dissipation of the LNA is simulated as 830-µA at 1-V supply voltage. The simulated return loss at the input is 27 dB at 404-MHz and whereas it is 27 dB at the output. The simulated small-signal gain at 404 MHz is around 12 dB. The isolation between the input and the output is better than 42 dB. The NF at the band is simulated as 1.25 dB. The input 1-dB compression point is -21 dBm. The input third-order intercept point of the LNA, with the fundamental RF signal at 404MHz and a second tone at 403MHz, is -11dBm.

3. Measurement Results

Figure 5 shows the micro-photographs of the differential CMOS LNA. The input and output matching components are placed on the test board. Figure 6 shows the measured small-signal gain of the differential LNA after the component losses have been de-embedded. The differential LNA draws 830 µW of power from a 1-V supply while providing a small-signal gain of ~12 dB at 404 MHz. The input return loss is 25 dB whereas the output return loss is 18 dB. Figure 7 had the de-embedded noise figure plots. The noise figure at 404 MHz is 1.32 dB.

Figure 8 shows the 1-dB gain compression point measured with the spectrum analyzer. The gain of amplifier compresses 1dB at -21.7 dBm of input power. The input third-order intercept point is measured -9.7 dBm with 1MHz offset signal.

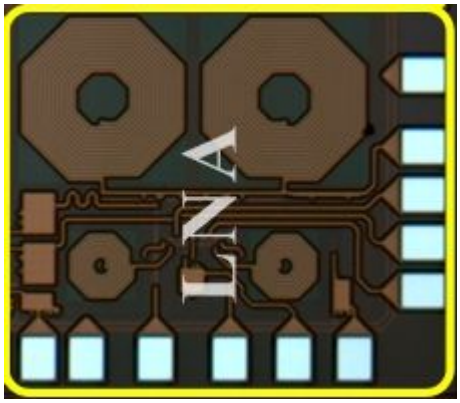

Fig. 5. Micro-photograph of the fabricated CMOS Differential LNA.

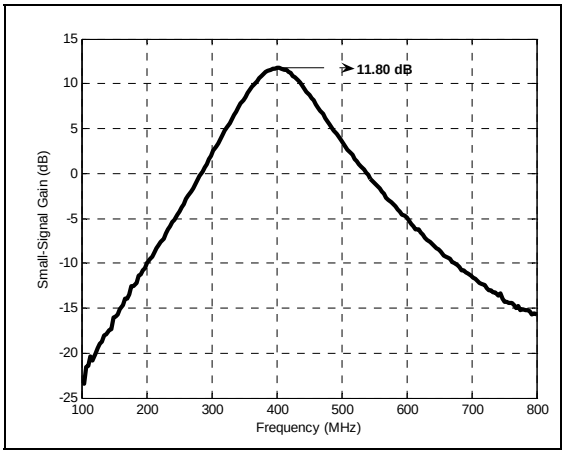

Fig. 6. Measured small-signal gain of the Differential LNA

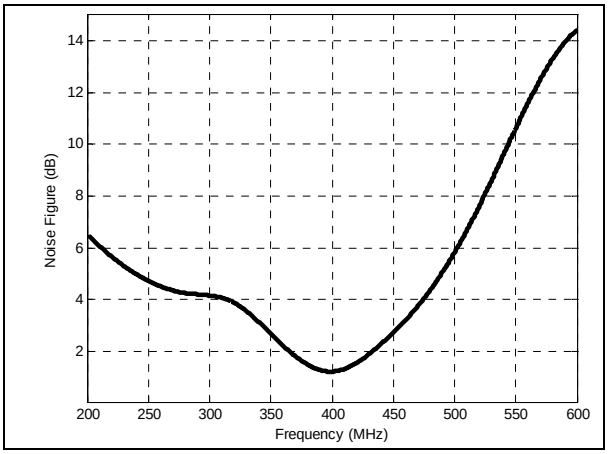

Fig. 7. De-embedded noise figure measurement response of LNA

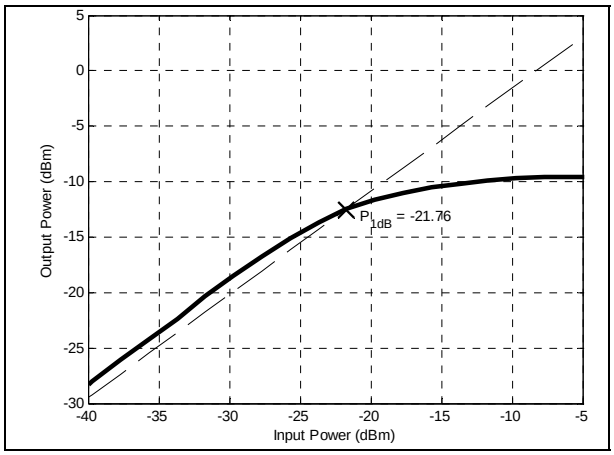

Fig. 8. Gain compression of Differential LNA

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4. Conclusions

The design of a differential CMOS LNA used in Medical Implant Communication Systems is presented in this paper. The die-level EM simulation is utilized on the passive inductors to account for the parasitic capacitance, resistance and inductance coming from the layout. It gives more insight for the designer to account for such unwanted effects. The simulation and measurement results of the circuit show a close correlation.

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