Topological and Functional Partitioning in EM Analysis: Application to Wafer-Level Chip-Scale Harmonic Filters

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***Abstract*— Aggressively applied function and geometry oriented partitioning is proposed for design and analysis of RF harmonic filters. The efficiency of the proposed methodology is demonstrated by application to the RF portion of an NXP semiconductor transceiver design. Simulation is compared to measurement at both component and function-block levels. Limits of partitioning assumptions in comparison with full-electromagnetic model approaches are discussed. Guidelines and design rules for partitioning of scalable multi-port sub-structures for back analysis in circuit simulator frameworks are studied.**

***Index Terms*—Electromagnetic analysis, method of moment, Functional and Topological Partitioning, internal ports.**

I. Introduction

In chip-scale-packaging and wafer-level-packaging, advanced integration solutions are being investigated to integrate formerly external passive devices on chip. However, they face real modelling challenges.

At chip scale, capacitive and inductive couplings [1-3] used to be addressed from schematic driven analysis supported by designers' experience and iterative trial and error. Schematic driven methodologies lead to first order simplifications that are useful for initial guess analysis. However, they fail to predict critical couplings caused by layout specific parasitics. In order to account for layout parasitics, electromagnetic (EM) analysis is required. However electromagnetic analysis of an entire chip is not possible with existing EM tools because of the complexity of layout details even when computer clusters are used. In order to realize EM accuracy analysis at the system level, methodologies are required to detect performance-limiting factors early in the design cycle.

This paper explores both a geometric based and a functionality based partitioning, or divide and conquer, methodology for the design and optimization of chip-scale-packaging and wafer-level-packaging. The accuracy of these methodologies is evaluated in comparison to global electromagnetic simulation and to measurement, yielding suggested guidelines.

While divide and conquer is a time-honored technique, the advent of perfectly (i.e., to within numerical precision) calibrated ports [4] and [5], both on the edge of a circuit and completely internal to the circuit and remote from any possible global ground reference, now allows application of this approach in an aggressive manner never before thought possible. To illustrate an aggressive divide and conquer we consider the RF filter portion of a complex RFIC receiver.

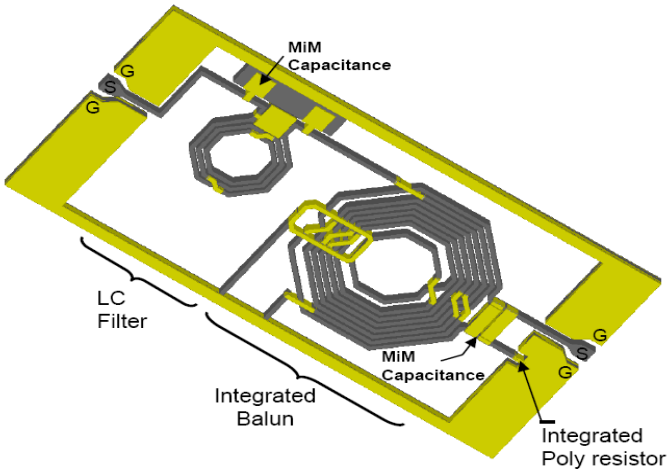

Fig. 1. RF filter circuit composed of a LC filter, a balun component and a poly-resistor termination with seal-ring grounding.

The approach is illustrated here with simple structures so that global EM analysis remains feasible. Application of divide-and-conquer methodology to co-design and co-analysis of multi-level Chip-Package-Board can be facilitated by coupling full-wave EM analysis (for critical circuit portions) with quasi-static solutions.

II. Application, Correlations Analysis and Discussions of Main Results

A. Description of Carrier Application and Partitioning Strategies

EM analysis with the method of moments (MoM) divides the surface of conductors into subsections. For N subsections, the moment matrix memory is proportional to N^2 and the matrix solve time is proportional to N^3. If the structure is divided into two substructures of ½ N each, memory is reduced by ¼ for each substructure, and the total matrix solve time for both substructures is about $^1/_8 + {}^1/_8 = ¼$ of the solve time. Matrix solve time is typically the limiting factor. The example presented in this section is a balun with integrated poly resistor termination and LC filter, Fig.1.

Dividing a circuit layout into sections means that electromagnetic coupling is considered within each section, but not between sections. Interaction between sections takes place only through the connecting ports, there is no fringing field coupling between sections. This is the reason why divide-and-conquer cannot be applied in some situations. It is limited to those cases where most of the fringing field

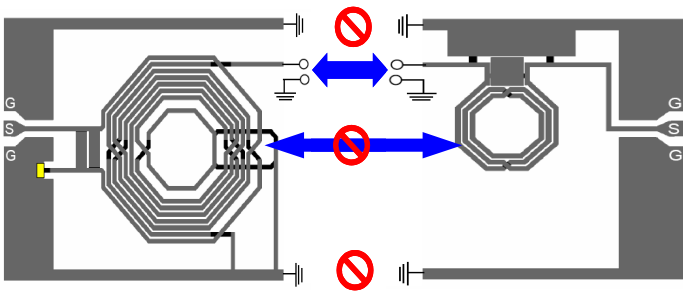

Fig. 2. Subcircuit division with local grounds connected to global ground, thus enforcing one specific mode.

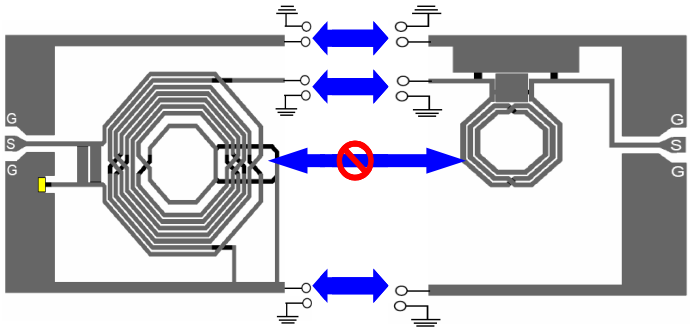

Fig. 3. Sub-circuit division with ports for each conductor, giving the EM solver additional degrees of freedom to find the physically correct solution.

coupling is local and far cross-talk is not an issue. Typical applications are circuits where the circuit size is much larger than the distance between signal lines and ground return path.

For silicon integrated circuits, there is typically no global ground. Rather, any ground strips (CPW) in place on top of the substrate and induced current in the conducting substrate form the ground return path. The only way to excite ground return current is to excite a signal current. In EM analysis, the signal current is excited by means of a port.

The ports between the sections of a circuit must give the EM solver enough degrees of freedom to excite all possible combinations of signal and ground return currents as needed. When ports are placed only on "signal" lines that cross a section boundary, Fig.2, all ground strips are connected to the global ground of their section. If there is more than one ground return path (don't forget the conducting substrate), then the distribution of total ground return current between the multiple paths in each section is likely different in the entire circuit. Thus, one should always define ports for all conductors that connect section boundaries, Fig. 3. Remember that ground return is an arbitrary human convention. Electric current does not care what we call "ground", and section port selection should reflect this fact. For the used EM method, extra ports typically have minimal impact on analysis time.

To apply the partitioning approach successfully, a very accurate port calibration technique is required. By analyzing a circuit layout in pieces and connecting results with nodal analysis, even a circuit with only two external ports can require a large number of ports for re-connecting the individual sections. In Fig. 4, the circuit is divided into five sections, with a total of 73 additional ports.

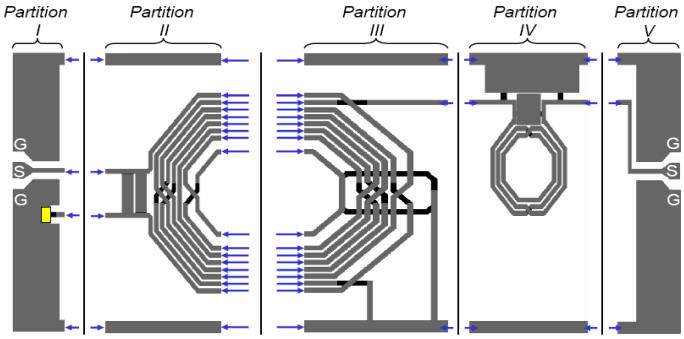

Fig. 4. Geometric subcircuit division into five pieces. Total number of box wall ports used to connect the pieces is 73.

The effect of errors from bad port calibration might not be obvious when there are few external ports and no internal ports, but any port calibration error becomes apparent when a large number of ports are cascaded for the divide-and-conquer approach. It can be seen from Fig. 4 that one cutting plane divides the balun into two pieces, which are then connected through a large number of ports.

This was done to demonstrate that partitioning can be applied even on a component level if a cutting plane can be found where EM coupling between sections is minor.

The savings in simulation time and memory requirement achieved with this partitioning is significant, leading to a 6x faster analysis.

The divide and conquer with simple straight section boundaries discussed above is based on the geometry; it does not consider functionality. One reason to use geometric circuit division is that it can be automated. Once the user has defined section boundaries, the sections are created with the appropriate port number and reference planes, together with a netlist that re-connects all sections and calculates the overall circuit response.

Functional circuit division requires knowledge of the circuit. Fig. 5 demonstrates a simple functional division into a frame with coplanar feed structures and terminations, the balun, and the filter. A typical functional division can be to separate the interconnect network from the components. One benefit is that different simulation settings can be used for the different sections, like a refined mesh for critical components, and a fast coarse mesh for the interconnect. For this example, all sections have been simulated with identical mesh settings. Another benefit of functional division is that section results can be interpreted easily, and previously simulated sections are easily re-used. Finally, circuit sections in the functional division that represent individual components might be extracted as scalable models.

Functional division requires calibrated internal ports, because port locations for connecting some circuit sections can be distributed on the interior of other, larger, circuit sections, far from any global ground that might be used as a port reference. To handle this complicated port arrangement with the required accuracy, co-calibrated internal ports [4] with a floating local ground reference are used.

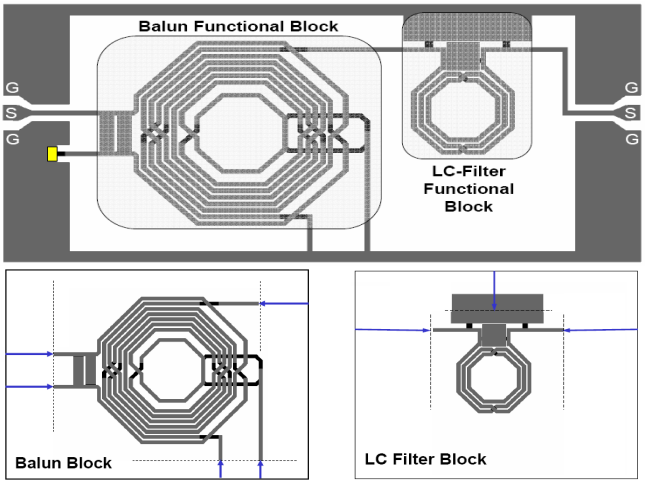

Fig. 5. Functional division into three sections, the first section containing internal co-calibrated ports with floating ground references, ready to receive the result of the second and third sections..

TABLE I: SIMULATION TIME AND MEMORY REQUIREMENT (ON DUAL XEON 5420)

	Full-Analysis	Functional Divide-and-Conquer Three Sections (S_1, S_2, S_3)		
		S_1 Balun	S_2 LC-Filter	S_3 CPW-Seal
Memory Storage	1001 MB	221 MB	47 MB	99 MB
CPU Time	66 min total time	5 min	1 min	6 min
		Overall time = 13 min total incl. combine		

The savings in simulation time and memory requirement achieved with this functional division is significant, as shown in table I. However, preparing the functional circuit sections must be done manually, while the geometric division can be highly automated.

B. Validations and Correlation with Measurement

In Fig. 6(a), (b), the results of the geometric and functional division are compared to full-circuit simulation. The results are nearly visually identical over the full band from 100 MHz to 9 GHz for both magnitude and phase of all S-parameters.

Some differences are discernable near 2 GHz, and between 9GHz and 10GHz. For the geometric subdivision, difference from the full analysis is 0.01 dB in the pass band insertion loss and 20 MHz in pass band frequency. For the functional subdivision, the difference is 0.09 dB in the pass band insertion loss and 10 MHz in frequency.

The degree of agreement between the full analysis and the sectioned analysis confirms that crosstalk between the sections is small for this example, and partitioning is correctly applied. Of course, that might not be known a priori, in which case, a simplified test case can estimate the amount of crosstalk between sections as in the first example in this paper.

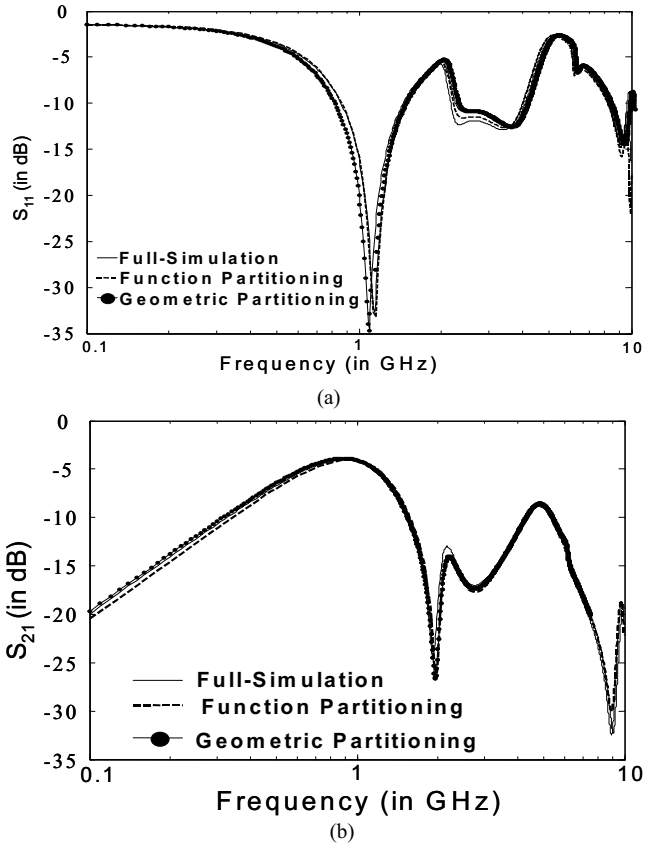

Fig. 6. Magnitude of S_{11} and S_{21} of the full EM analysis compared to functional and geometric circuit subdivision.

For the example immediately above, a crosstalk analysis was performed and gave a crosstalk level of -20 dB or better, relative to the wired signal level, in the frequency range up to 7 GHz. The only exception was a narrow frequency band around 2 GHz where the crosstalk was as high as -10dB relative to the signal level. This matches the results of the full analysis vs. sectional analysis where deviations are seen in that frequency range. Above 7 GHz, crosstalk between the sections increases and reduces the accuracy of the sectional analysis. In Fig. 7, the simulation results are compared to measurements. The difference between measurement and the full simulation is 0.3 dB in the pass band insertion loss and 50 MHz in frequency. A small difference in insertion loss is seen in the frequency range 2.5 – 6 GHz. The reason for that difference is unknown at the present time.

For the geometry based partitioning of the transceiver example, one cutting plane divides the transformer into two pieces, to demonstrate that partitioning at component level is feasible. To get accurate results, each cutting plane must be chosen with care. This is shown with another test case, where a transformer is partitioned in three different ways. Partitioning a simple element like a transformer might seem overkill, but this is a useful step on the way towards hybrid tuning methodology [5] and scalable models. The sections of the transformer can now be used as building blocks, to compose a whole family of new transformers.

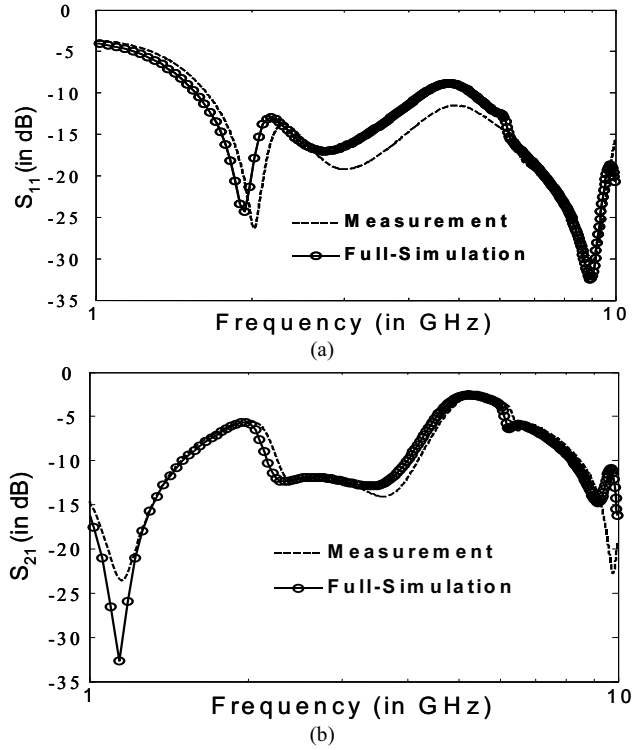

Fig.7. Magnitude of S_{11} (a) and S_{21} (b) of the full EM analysis compared to measurements

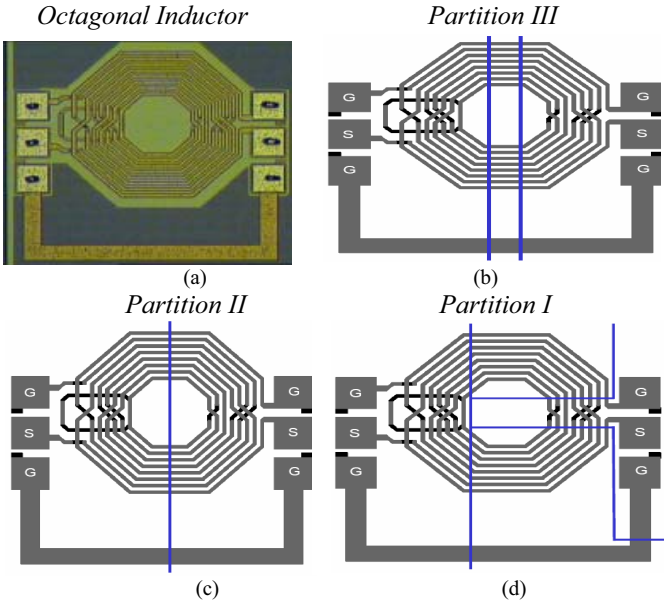

Fig.8. Photographs of measured 8-turns transformer (a), *Partition III (b), Partition II (c)* and *Partition I (d)*. S_{11} (a) and S_{21} (b) parameters for the measured 8-turns transformer.

The three different partitioning strategies for the transformer test-case are shown in Fig. 8. For partitioning strategy II and III, the cutting plane is located in the horizontal sections, where all conductors are perpendicular to the cutting plane. This ensures that in the EM analysis of each piece, where port feed lines are added at the cutting plane, the current flow and thus the fields are very similar to the original circuit.

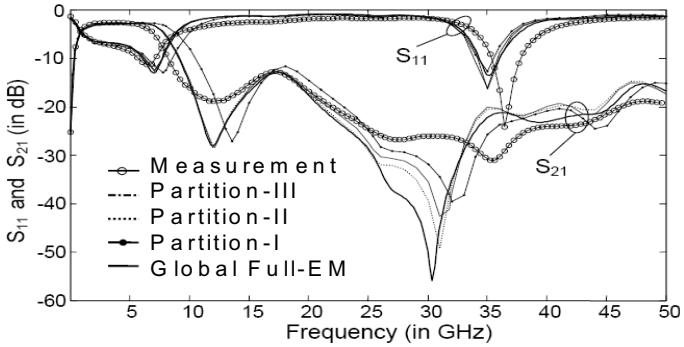

Fig.9. Comparison between full-wave single global model, 3 different partitioning strategies and measurement.

For strategy I, the cutting planes are located on the diagonal segments. In this case, the cutting plane is not perpendicular to the conductor segments, and the port feed lines in the piecewise analysis point into other directions than the conductors in the original circuit. This means that the fringing fields at the cutting plane are different between the pieces and the original model. Simulation results in Fig.9 clearly show that partitioning was carried to far in this last case.

III. Conclusion

Divide and conquer is a traditional approach to simplifying complex microwave circuit analysis problems. However, in the past it has been applied cautiously, always minimizing the number of additional ports used to re-connect the sections of a circuit. In addition, the sectional ports are carefully placed in non-critical locations in traditional microwave systems. Because of the advent of perfectly calibrated (i.e., to within numerical precision) ports in EM analysis, divide and conquer can be used very aggressively as illustrated here with application examples, using a much larger number of ports, even within critical parts of the signal path. This type of partitioning approach, which is easily applied to much larger circuits, enables the efficient and accurate analysis of the large and complicated high frequency and high speed systems now being designed. At component level, partitioning enables a building block approach where a family of new components can be derived from the analysis.

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