Application Notes

Accurate Modeling of Monolithic Inductors Using Conformal Meshing for Reduced Computation

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One distinction of Si/SiGe BiCMOS and radio-frequency-enabled CMOS (RF CMOS) in comparison to traditional digital CMOS is the increasing availability of high quality factor (Q) passive components. A great deal of attention has been focused on improving the Q factor of monolithic inductors on silicon, which can suffer from parasitic effects due to low substrate resistivities in bulk CMOS technologies [1]–[3]. Low Q factor inductors result in lower gain in amplifiers, greater insertion loss in matching networks, and higher phase noise in oscillators. As a result, thick "analog" metal layers have been added to back end of the line (BEOL) processing in RF-enabled Si technologies to facilitate higher Q inductors.

Accurate component modeling is a key factor to successful wireline and wireless circuit design in Si/SiGe BiCMOS and RF CMOS. For example, in recent years, circuit designers have come to rely heavily on electromagnetic analysis to properly account for parasitics and optimize the design of inductors used in a particular circuit. It is obviously desirable to sweep parameters, such as coil spacing and trace width, in order to maximize Q for a given effective inductance in a particular technology [4]. However, complex inductor designs are difficult to optimize since they require large amounts of memory and long simulation times.

Moreover, the closely spaced thick metal layers of modern monolithic inductors pose a significant challenge to electromagnetic simulators. As will be shown in this article, planar electromagnetic simulators need to employ multiple layers of thin metal sheets separated by dielectric layers to reproduce the effects of tightly coupled thick metal traces. Unfortunately, these multiple metal layers increase the mesh density and, therefore, the simulation time per frequency point. The problem is similar for full three-dimensional (3-D) electromagnetic simulators since, for full accuracy, the volume mesh size must be small compared to the thickness of the metal.

This article presents the application of two planar electromagnetic simulation methods for reducing the memory and computation time requirement for accurate simulation of inductors fabricated with thick analog metal layers. First, a "conformal" subsectioning technique is briefly discussed in the context of reducing the numerical complexity of octagonal and circular spiral inductor analysis. Second, this article discusses a method for determining if more than a two-sheet model of thick metals is needed for accurate inductor simulation. Finally, the conformal mesh is applied to a 3.3-nH inductor fabricated using the IBM 0.13-μm RF CMOS process technology. The simulated and measured results are compared.

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Conformal Mesh

Simulation time can be reduced in planar analysis by increasing the size of or combining multiple subsections. Unfortunately, this is usually not an option in complex components or circuits, such as monolithic inductors, because the use of fewer subsections reduces accuracy. This is especially true for the edge current of inductors, which requires a very fine mesh for accurate results.

A common way to reduce cell counts in electromagnetic analysis is to use rooftop functions, which linearly weight and

combine neighboring subsections [5]. Accuracy is maintained by limiting the width of large rooftop sections at the edges of the conductor, where the majority of current resides due to the edge effect. Since combined rooftop subsections must be rectangular, this meshing scheme is ideal for Manhattan geometries (i.e., structures that only contain 90° angles, like the streets of Manhattan, New York) but offers little improvement for continuous octagonal or circular inductor spirals.

Recently, a technique for combining multiple subsections while maintaining high-edge current information has been implemented for nonrectangular, or non-Manhattan style geometries [6]–[8]. This technique is called conformal meshing because the combined subsections can conform to arbitrary curves in the conductor. For octagonal and circular inductors, conformal meshing allows a significant reduction in subsection count, and, therefore, in memory and simulation time.

As with rooftop-combined subsections, conformal subsections have limited width near the edges of the conductor, so the high edge current information is maintained. In fact, results obtained from conformal subsectioned circuits are almost exactly identical to using a small rectangular or diagonal mesh. Thus, accuracy is preserved while dramatically reducing the memory and analysis time requirement for complex geometries.

Thick Analog Metal Layers

A simple way to model thick conductors in planar electromagnetic simulators is to use two sheets of infinitesimally thin metal separated by a dielectric with the same thickness as the metal. Accuracy can be improved by increasing the number of sheets sandwiched between the uppermost and lowermost metal layers. However, as mentioned previously, this improvement comes at the expense of simulation time due to increased mesh density. Increasing the number of sheets increases the capacitance per unit length between sheets and reduces the self-inductance per unit length. The results are extrapolated to the infinite sheet case for the inductance and capacitance per unit length.

When the thickness of the metal is greater than the spacing of the inductor coils, more sheets of metal are required for accurate simulation because the capacitance per unit length and inductance per unit length change drastically from a two-sheet model to the infinite sheet case. Physically, the interwinding capacitance of the inductor is not well accounted for in the planar simulator until more sheets of metal are used. However, if the coil spacing is larger, a two-sheet model may be sufficient to account for the interwinding capacitance of the coils. It is useful to know if a complex model using multiple sheets is required before the inductor is fully simulated.

The change in capacitance per unit length and inductance per unit length from the two-sheet case to the infinite sheet case can be used as a gauge to indicate whether or not the ratio of the coil spacing to the metal thickness for a particular inductor geometry warrants the added complexity of a several-sheet model for thick metal in planar electromagnetic simulators. A large change in capacitance per unit length and inductance per unit length as the number of sheets increases indicates a need for either multiple sheets or the application of a space-mapping layer to model the inductor [9]. Space-mapping layers have permittivities and permeabilities appropriate to make the capacitance per unit length and inductance per unit length of the simple two-sheet model exactly match those of the thick metal case. On the other hand, a small change in capacitance per unit length and inductance per unit length as the number of sheets increases means that a two-sheet model may return similar results to a model with many sheets, but requires far less computation time.

The capacitance and inductance per unit length of the thick metal is found by running several simulations of a coplanar waveguide (CPW) transmission line with the same width (w) and gap (g) as the spiral inductor to be simulated. These simulations alone do not model the current in the actual inductor exactly, since current is forced to the odd mode in the CPW. However, it is assumed that even mode currents are relatively unaffected by metal thickness, and relatively unaffected by multiple sheets of metal. The total current in the inductor is a sum of the even and odd mode currents; therefore, to reduce simulation complexity, only the odd mode currents are considered to determine the relative change in capacitance per unit length and inductance per unit length as the number of sheets increases.

Ideal, lossless metal is used for these simulations. Each iteration of the CPW simulation increases the number of sheets while keeping the distance between the upper and bottom sheets the same as the total thickness of the analog metal. The capacitance and inductance per unit length are calculated for each simulation to show the trend toward the infinite sheet case. Capacitance per unit length is given by:

$$C' = \frac{\sqrt{\varepsilon_{\text{eff}}\mu_{\text{eff}}}}{Z_0 \cdot c} \tag{1}$$

and inductance per unit length is given by:

$$L' = Z_0 \frac{\sqrt{\varepsilon_{\text{eff}}\mu_{\text{eff}}}}{c} \tag{2}$$

where $c = 2.99792458 \times 10^8$ m/s (exactly) is the speed of light in a vacuum, Z_0 is the characteristic impedance, ε_{eff} is the (relative) effective dielectric permittivity, and μ_{eff} is the (relative) effective dielectric permeability (Z_0 and ε_{eff} are calculated in the simulator and reported back, with the quantity reported as ε_{eff} really being the product of ε_{eff} and μ_{eff}).

The advantage of simulating the CPW structures and evaluating the change in capacitance per unit length and inductance per unit length is that this requires far less time to simulate than a full inductor, but still provides the ability to determine the relative benefit of increasing the number of sheets used to model thick metal. As a benchmark, a simulation of a nine-sheet, 2.5-turn, 200-μm outer diameter inductor requires approximately 45 min per frequency on a 3-GHz Pentium. A corresponding nine-sheet CPW simulation requires only 1 min, 14 s per frequency on the same system. Therefore, CPW simulations performed before the inductor simulation offer the potential for substantial time savings, if it is determined that a two-layer model will suffice.

If the two-sheet model is determined to be acceptable, the inductor simulation is then set up by creating two metal sheets separated by a dielectric layer equivalent to the thickness of the analog metal. Conductor loss in the inductor is simulated by modeling each sheet of metal with the thin-film conductivity and half the total thickness of the actual metal layer.

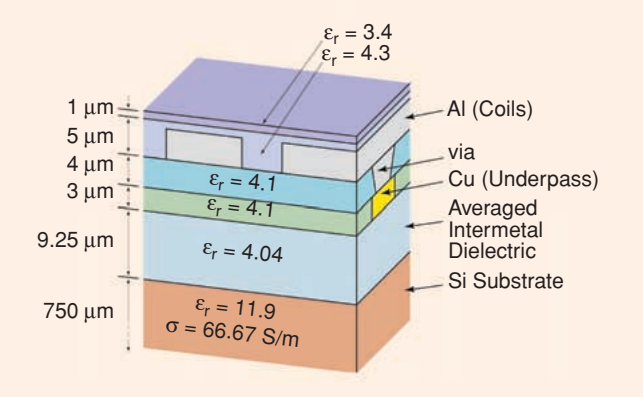

Figure 1. *IBM CMRF8SF high-Q factor inductor cross-section with the weighted average dielectric constants and layer thicknesses used in the simulator.*

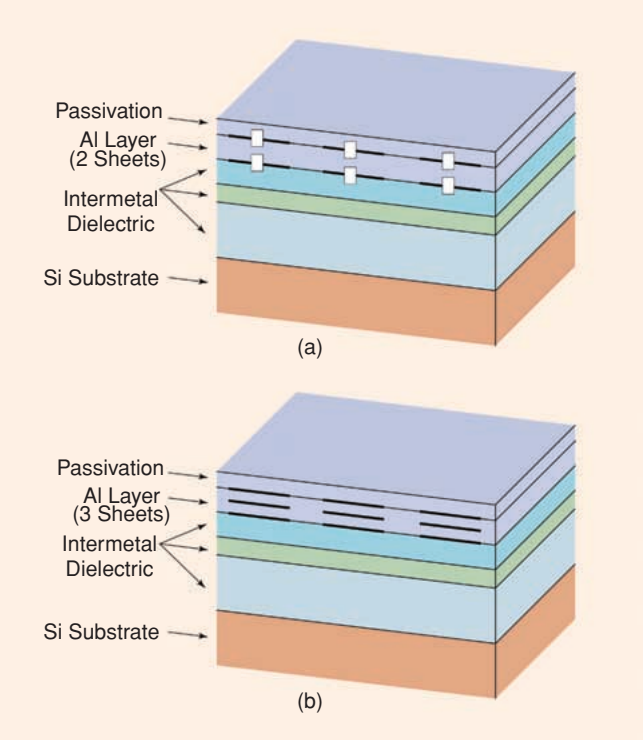

Figure 2. *CPW cross-section for the 4-µm aluminum layer. (a) Two metal sheet base case. (b) Three metal sheet case.*

RF CMOS Application Example

An octagonal inductor is fabricated in IBM's 0.13-μm CMRF8SF technology with a 3-μm thick next-to-last copper layer and a 4-μm thick aluminum last metal layer. The monolithic inductor coils are laid out in the 4-μm aluminum last metal and the 3-μm copper is used for the underpass (Figure 1). The 3.5-turn octagonal inductor in this example has an outer diameter of 200-μm, a coil trace width of 5-μm, a coil spacing of 5-μm, and an underpass trace width of 15-μm. These dimensions result in an effective inductance of approximately 3.3 nH at the peak Q factor around 5.5 GHz.

A set of CPW simulations are performed for the 4-μm thick aluminum layer. Since the copper layer is used for the underpass and not for any of the inductor coils, the CPW simulations are not necessary for the copper layer. The simulations start with two sheets of metal. For each iteration, the number of dielectric layers between the uppermost and lowermost metals are doubled, resulting in cases with two, three, five, and nine metal sheets. Figure 2 shows an example of the two- and three-sheet cases for the aluminum layer. Input and output ports of the CPW use matching port numbers on each layer of metal (e.g., on the Port 1 side of the CPW, a port is placed on each individual stacked sheet of metal and assigned Port Number 1). A corresponding negative port number is placed on the ground connecting lines of the CPW on each metal sheet to enforce all ground return current to flow over the CPW ground strips.

Table 1 shows the capacitance and inductance per unit length results for the aluminum layer. Since the capacitance and inductance per unit length do not change significantly by increasing the number of sheets for the aluminum layer, a two-sheet model is selected for the aluminum layer in the inductor simulations. The validity of this assumption will be verified by comparing the simulated results to the measurements of the fabricated inductor. A two-sheet model is also used for the 3 μm thick copper underpass.

Figure 3 shows a 3-D view of the two-sheet per thick metal layer model of the inductor. The aluminum and copper layers have thin film resistivities of 2.80 $\mu\Omega$/cm and 1.80 $\mu\Omega$/cm, respectively, and are given thicknesses in the simulator of half the total thickness of the layer to properly account for conductor loss in the combination of the two sheets. Ideal, lossless vias are added at each half turn of the inductor to connect the two sheets of metal, keeping the current density in the two sheets synchronized throughout the turns of the inductor.

Regular and conformal meshing are used to simulate the

Table 1. Capacitance and Inductance per unit length in the CPW simulations of the aluminum layer.

Sheets	ε_{eff}	Z_0	L/m	C/m
2	3.67	59.56	3.81E-07	1.07E-10
3	3.69	57.31	3.67E-07	1.08E-10
5	3.69	56.57	3.63E-07	1.09E-10
9	3.70	56.37	3.61E-07	1.10E-10
infinite case (extrapolated)	3.70	56.29	3.61E-07	1.10E-10

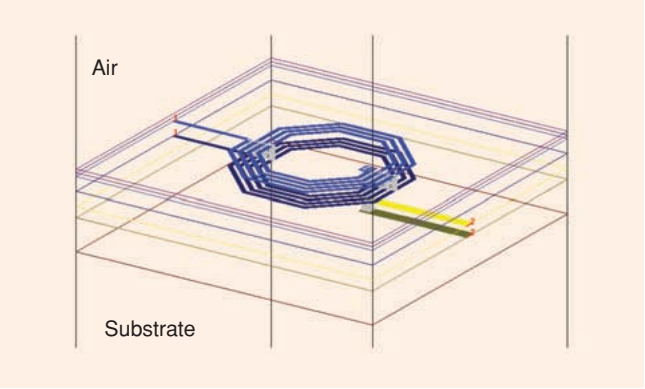

Figure 3. *3-D view of the two-sheet per thick metal layer model of the 3.3-nH inductor.*

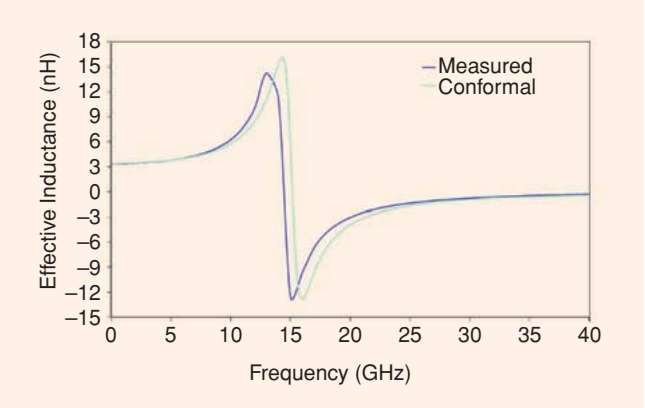

Figure 4. *Measured effective inductance compared to conformal mesh simulations of the inductor.*

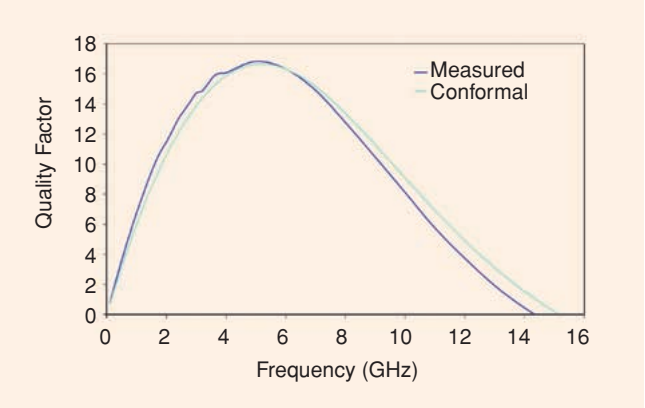

Figure 5. *Measured Q factor compared to conformal mesh simulations of the inductor.*

Table 2. Comparison of simulation times and memory requirements using conformal and regular mesh schemes. Data reported from a 3-GHz Pentium system.

Mesh	Simulation Time per Frequency	Memory
Conformal	12 s	22 MB
Regular	42 s	96 MB

monolithic inductor. As shown in Table 2, the conformal mesh simulation requires about 1/4 the memory and under 1/3 the time per frequency of the regular mesh simulation.

Since this inductor is intended for single-ended use, the effective inductance is calculated from two-port measurements using [3]

$$L_{\text{eff}} = \text{Im}\left(\frac{1/Y_{11}}{2\pi f}\right) \tag{3}$$

and the Q factor is calculated using

$$Q = \frac{\text{Im}(1/Y_{11})}{\text{Re}(1/Y_{11})}. \tag{4}$$

The fabricated inductor was measured using an on-wafer probe station. An Alumina calibration standard substrate is used to perform a SOLT calibration to the probe tips. The calibrated probes are used to measure the inductor structure and a set of pad deembedding structures. Before the results can be compared to the simulated data, the probing pads are deembedded from the measured S-parameters [10]. Without deembedding, the measured S-parameters would yield a lower self-resonant frequency and lower Q factor due to the added parasitic shunt capacitance and series loss of the pads.

Figure 4 compares the results of the conformal mesh simulations with the measured effective inductance. In the linear portion of the inductance curve, the conformal mesh simulated data is within 1% of the measured effective inductance. The self-resonant frequency of the conformal mesh simulation is within 5% of the measured data. As predicted by the small change in capacitance per unit length and inductance per unit length in the CPW simulations, the combination of the two-sheet model and conformal meshing returns results very close to those of the measured inductor.

Figure 5 shows the measured and simulated Q factor. At the peak, the conformal mesh simulated Q factor is within 1% of the measured data. The conformal mesh curve follows the same trend as the measurements at higher frequencies beyond the peak Q factor, but is slightly higher than the measurements. Better high frequency (i.e., beyond 7 GHz) correlation with the measured data can likely be obtained by including the ground strips that surround the fabricated inductor in the simulation model. These ground strips are omitted in the electromagnetic simulation to simplify the model and reduce memory requirements. In the actual inductor, the ground return current can flow in either the CPW ground strips, or in the substrate ground plane on the bottom side of the silicon (the ground strips are connected to the ground plane by vias). Without these ground strips, the ground-return current flows either in the lossless box sidewalls, or in the substrate ground plane. Thus, the model being analyzed is physically different from the component that was measured, but it appears to have only a minor effect and only at frequencies beyond 7 GHz.

The regular mesh and conformal mesh results are nearly identical, so they are omitted from the graphs for clarity. Since the regular mesh requires approximately three times the simulation time per frequency, the conformal mesh translates

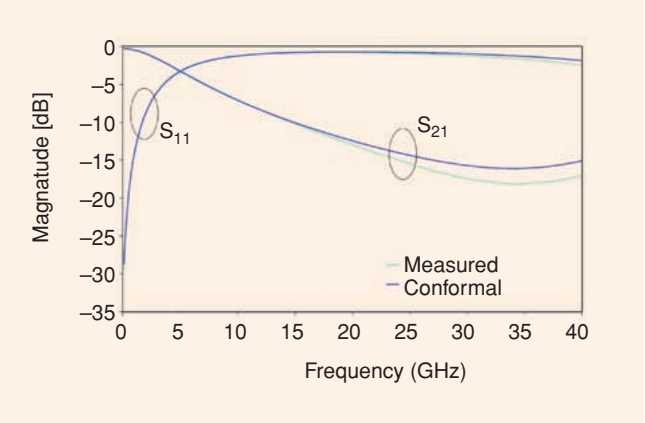

Figure 6. *Plots of the magnitude of S_{11} and S_{21} obtained from measurement and from conformal mesh simulation.*

to a tremendous time savings, with virtually no difference in the simulation results.

The correlation between measured and simulated Q factor and effective inductance supports the selection of a simple two-sheet model for the thick metal layers in this example inductor. It should be noted that inductors with wider traces spaced closer together would require a more complicated model than the two-sheet model used for this inductor. This would be revealed by the use of the CPW pre-simulations described above, thus saving unnecessary extra simulation time.

Figure 6 is a plot of the magnitudes of S_{11} and S_{21}. The 1% error at the peak of the conformal mesh simulated Q factor is a result from small differences in the S-parameters. At 5 GHz, the conformal mesh simulated S_{11} is 0.8 dB higher than the measurement at –3.36 dB. The conformal mesh simulated S_{21} is 0.8 dB lower than the measurement at –3.16 dB. Q factor is affected by these small differences more than effective inductance because Q factor is calculated as a ratio of the S-parameters and effective inductance is calculated by scaling the S-parameters [see (3) and (4)].

Conclusion

Conformal meshing is used to accurately simulate an inductor fabricated in the IBM 0.13-μm RF CMOS process technology. Effective inductance is simulated within 1%, and the self-resonant frequency is simulated within 5% of those of the measured inductor. The peak Q factor is simulated within 1% of that of the measured inductor. Since the coil spacing

of this inductor is larger than the metal thickness, and the traces are relatively thin, a simple two-sheet model of the analog metal layers in this inductor is sufficient to reasonably match measured results. However, a technique is described that allows designers to check the number of sheets needed without full inductor simulation.

The conformal mesh simulations require approximately 1/3 the simulation time per frequency on a 3-GHz Pentium of the regular mesh simulations of the same inductor. In general, conformal mesh should be used when the layout has non-Manhattan geometries that would otherwise prevent subsection combination. Conformal meshing allows accurate modeling of complex monolithic inductors to be more efficient by dramatically reducing simulation time. Furthermore, conformal meshing allows efficient sweeps of inductor parameters for optimization purposes that would otherwise be prohibitively long.

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