Shortening the Design Cycle

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Electromagnetics (EM) has today become a critical part of the microwave design cycle. This article briefly traces the entry of EM into microwave design and describes how today's design cycle arose. Then, we discuss how recent developments (in particular, perfectly calibrated ports in EM analysis) open entire new areas of applied microwave design.

Typical products resulting from the new EM-based methodologies are shown in Figure 1 from Dielectric Labs [1]. While these filters look like normal two- and three-port structures, the EM analyses for these filters using the new design methodologies (topological partitioning, functional partitioning, and tuning methodology) typically include dozens of extra ports. Properly included, these extra ports reduce the design process from weeks and months to, literally, days. In fact, analyzing these filters as simple two or three ports is now sometimes a waste of time. As we describe the new design cycle below, you will see why this is happening. All of these new methodologies effectively amount to producing precisely and quickly *tunable* EM analyses.

Background

Twenty-five years ago, when I started my company (Sonnet Software) [2], numerical EM had virtually no mindshare in the microwave and high-frequency design community. Back in the 1970s, the design cycle started with a Smith Chart and slide rule. Later on we started using calculators and circuit theory software on

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computers. After designing, we would build it and measure it. Usually, the circuit did not meet requirements, so we had to redesign. For circuits with large dimensions (i.e., you could actually see the circuit), redesign could sometimes be done with an exacto knife and silver epoxy. Toward the end of my hardware days, I started designing some of the first gallium arsenide microwave integrated circuits. No exacto knife now and fabrication for each design iteration was three to six months and US$50,000.

This is when I started thinking that there has to be a better way. So I set off to Syracuse University, nailed down a Ph.D. [3], [4] under Prof. Roger Harrington [5] [the originator of the method of moments (MoM)], and changed the design cycle.

The new design cycle, still in wide use today, is to design the circuit using the usual circuit theory tools, just like we always used to back in the 1980s. Today, instead of building the circuit, the layout is passed to an EM analysis tool. For aggressive designs, the circuit still does not meet requirements. The redesign takes place entirely on the computer without the assistance of an exacto knife. You just modify the polygons of the layout. A complete redesign and EM analysis of a moderately complex circuit can now take a week or so, instead of the few months sometimes required by design-fabricate-measure.

Most of that week-long cycle deals with design closure. Because of the EM analyses, we know that our first layout will not meet requirements. Design closure is the process of deciding which elements to change and how much to change them. In the design cycle described above, this question is left up to the experience of the engineer, or to automated EM-based optimization, to propose a potentially successful redesign. Wouldn't it be nice if we could compress this process down to one day?

Seems impossible. A moderately complicated circuit requires an overnight run for just one EM analysis. (This is by definition. For this discussion, we define a moderately complex circuit to be one that requires an overnight EM analysis.) We require lots of EM analyses in order to figure out the sensitivities of the various dimensions for redesign. Faster computers don't even help. Sure, we get faster computers, but then our circuits get bigger. A moderately complex circuit still requires an overnight run.

Getting the design cycle to go faster is actually easy. Just throw away all those messy, time-consuming sensitivity EM analyses. We will allow one, and only one, EM analysis of the complete circuit per design cycle so it goes nice and fast. Hold on, now we're running blind! How do we figure out what to change to get design closure? Before we get to that key point, let's go over some background on EM analysis.

Different Kinds of EM Analyses

First, we mention volume meshing EM analyses. There are both time-domain (i.e., analyze one time step after another) and frequency-domain tools. These tools are important and valuable components in any high-frequency designer's tool chest and I strongly recommend having both types. However, this article is about planar circuits. For most planar circuits [unless there is a significant three-dimensional (3-D) portion], volume meshers are slower or less accurate than just about any specialized planar tool, so I will not consider them here.

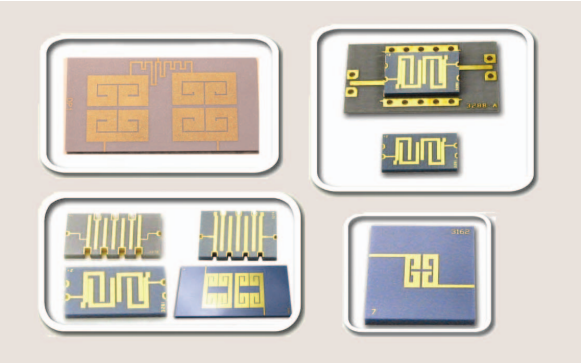

Figure 1. *Filters on ceramic designed by Dielectric Laboratories are the results of new microwave design methodologies that use numerous additional ports to facilitate rapid design closure.*

For planar surface meshing tools, there are two types: shielded and unshielded. Both tools mesh only the surface of the metal of your circuit into, say, N subsections. Then they both fill an $N \times N$ matrix and invert it. Matrix inversion is usually the limiting factor as it is order N^3. This is a common form of the MoM. Both approaches have their relative advantages and disadvantages and, again, I strongly recommend you have and use both.

Unshielded tools are based on a Green's function in an unshielded environment (the Sommerfeld integral), thus including radiation. The Green's function is integrated over four dimensions for each matrix element. For the Sommerfeld integral, this requires numerical integration, and answers are usually calculated to ± 0.001 or so. This accuracy is good enough for many applications. The advantage of the unshielded approach is that the numerical integration is easily performed over any size or shape subsection. This gives great flexibility in setting up the meshing of an arbitrary layout. The disadvantage is the ± 0.001. This is the tolerance on the numbers going into the $N \times N$ matrix to be inverted. For large matrices, inversion amplifies error. The larger the matrix (i.e., the finer the mesh), the more numerical issues arise. Because of this error issue, in situations using the new design cycle described below, unshielded tools are probably best avoided.

A recent development in unshielded EM analysis is fast techniques that are order $N \cdot \log(N)$ instead of N^3 as above. While commercially available for many years in fields like antennas and scattering, such tools have not seen application in microwave design due to inherent

low accuracy. Several vendors (Cadence, AWR, and Agilent) are now making serious attempts to improve the accuracy of these unshielded MoM tools for microwave circuit application. When a solid experience base is in place there is a possibility that such tools will render order N^3 unshielded tools obsolete. Let's watch carefully. Because such tools typically use an iterative matrix solve and approximate the Green's function (so that they are fast), these tools are unlikely to be appropriate for the new design methodologies we describe here. In addition, the $N \cdot \log(N)$ tools must do a complete iterative matrix solve for each port. If there are 100 ports, then matrix solve takes 100 times longer, which is highly undesirable for problems with large numbers of ports, which I describe below.

Shielded tools (i.e., the circuit is inside a shielding, conducting box) are based on a Green's function that is a sum of sines and cosines. The numbers that fill the MoM matrix are calculated to full numerical precision with a fast Fourier transform (FFT); there is no numerical integration. The down side to the shielded Green's function parallels digital signal processing. To do an FFT on a time signal, you must first uniformly time sample the signal. For shielded EM analysis, we must first uniformly sample the surface of the substrate. Thus, the analyzed circuit falls on a fine uniform underlying FFT mesh. This mesh can be very fine. For example a $1{,}000 \times 1{,}000$ FFT (which means the substrate surface is divided into 1,000 cells on each edge) requires one second on a typical computer. No more than three FFTs are required for a circuit with a single level of conductor. The FFT cell size for this case is approaching the pixel size in an HDTV screen. Even so, the disadvantage that shielded EM analysis has a uniform underlying FFT mesh remains.

The advantage for a shielded approach is that there is no ± 0.001 to worry about. Everything is done to full precision. This means meshing can be extremely fine and matrices can be extremely large without difficulty. To give some idea of matrix size and inversion time, I can invert a lossless $20{,}000 \times 20{,}000$ matrix in 14 minutes using 1.5 GB of memory on a 2.3-GHz dual core Centrino notebook. What frequency you are analyzing does not matter. How many ports you have does not matter. It is still 14 minutes. Those 20,000 subsections are composed of groups of the fine underlying FFT cells. The groups of FFT cells can be rectangular, or they can curve to follow curving geometries [6]. A circuit with 20,000 subsections could easily cover several million cells in the fine underlying FFT mesh. We can do some pretty complicated circuits with 20 million cells, and it is nice not having to worry about matrix solve precision error.

A key advantage of shielded analysis is that the perfectly conducting box sidewall provides a perfect ground reference for all ports on the edge of the circuit substrate. This, combined with full precision calculations, means we can do perfect port calibration. Ports in all EM analyses and in all physical measurements introduce error into the result. In a shielded analysis we use the box sidewalls as perfect short-circuit calibration standards [7]. In this way, the port error is perfectly characterized and removed. By perfect, we mean to with in numerical precision under the assumption that no port connecting lines are overmoded. Recently, we figured out how to do perfect port calibration on ports internal to the circuit, too (cocalibrated ports); even ports that have no access to anything like a global ground reference [8]. This development is critical to practical applied use of the new design cycle, especially when dealing with silicon.

Even very tiny port calibration error and Green's function (electromagnetic coupling) error can completely disable the new design methodologies we describe here. Fortunately, those two error sources are zero in a properly designed shielded EM analysis, leaving us only with error due to subsection size dominating. Error due to subsection size is typically on the order of 0.1% to 1.0% and its effect on the final outcome is also on that same order. We may now proceed.

Topological Partitioning

The new design cycle takes advantage of an old technique, divide and conquer, also known as partitioning. We are not talking about timid partitioning, say EM analyzing the amplifier and filter in separate analyses and then connecting them. We are talking about major surgery on the amplifier, filter, and everything else. We cut and hack away, and add in lots and lots of ports.

Lots of ports are key. With 50 or 100 ports in your formerly nice simple two-port circuit, every single port must be calibrated to high accuracy. Any port calibration error, especially when the ports are within high Q resonant portions of your circuit, threaten failure of the entire design.

How can you check to see if your favorite planar EM analysis can handle this? I recommend selecting a narrow-band filter. Split it into pieces. For the most sensitive test, the pieces should have lots of closely spaced ports. Now, EM analyze each piece, connect the pieces back together, and compare with an EM analysis of the entire filter. An example (Figure 2) is detailed in [9] and [10]. If you want to try this particular filter, it is part of the free SonnetLite [11]. Install SonnetLite and look in Help->Examples->Filters. SonnetLite interfaces directly with both Agilent ADS and AWR Microwave Office making it easy to test your new design flow just about anywhere. With the full version of Sonnet, partitioning is fully automated.

Splitting a filter in half, as in Figure 2, EM analyzing, and then connecting the pieces back together we refer to as geometrical or topological partitioning. The splitting must be done across the entire width of the circuit. This restriction is countered by the advantage that the entire process is easily automated. The only user input needed is on where to draw the splitting or partitioning lines.

As with all partitioning, no EM fringing field coupling across partition lines is included in the analysis. If fringing field coupling between partitions is important, this technique fails. For example, if the filter of Figure 2 is partitioned through the coupling region between two resonators (Figure 3) it cannot succeed. There can be problems if it is partitioned between the arms of a resonator, as the fringing coupling between the two arms is no longer included. For a general rule, transmission lines should be perpendicular to a partition boundary when they cross it. Transmission lines that are close to and parallel to a partition boundary can be a problem. (We have applied for a patent on a new, as yet unpublished, technique that includes coupling across partition lines, in which case the partitioning of Figure 3 works.)

With this restriction in mind, it is possible to successfully partition very aggressively, with Figure 4, from [12] showing the five sections into which the complete circuit on silicon from NXP was partitioned. One partition line actually splits the large spiral inductor in half. As described in [12], this extreme partitioning has almost no effect on the result. Note that the partition lines cross the entire circuit in Figure 4. This is important. There might be a temptation to not place ports on the ground lines (on the circuit edge) that cross the partition lines. If you partition manually, be sure to insert ports on each ground line. too. Otherwise, this approach can fail. The EM analysis and the current flowing on the ground lines really do not care what we call any of the transmission lines crossing the partition boundary. They all need to be treated just like signal lines.

Partitioning provides a speed advantage for order N^3 tools that fill and invert a matrix. By splitting the analysis in half, we reduce N by a factor of two, then matrix solve is reduced by a factor of eight. But with a circuit split in two, we must perform two EM analyses, each eight times faster, for a total gain of four times faster. Sometimes symmetry (as in Figure 2) allows us to use one analysis twice, giving us a full eight times advantage.

There is more to gain than speed. After partitioning and EM analyzing a circuit, one can now make certain changes quickly. For example, with the filter of Figure 2, you can increase the length of all resonators by connecting a multiple coupled line in between the two halves. The multiple coupled line can come from a good circuit theory model, or it can be generated from an EM analysis. Increase the length of the added line to decrease the center frequency of the filter. To shorten all the resonators, connect a *negative* length line. While not physical, circuit theory and EM analysis programs both have no trouble doing this. The size of the large inductor of Figure 4 can be easily modified as well. Just connect a multiple coupled line in between the two halves. No need to repeat the entire EM analysis. Tune up your layout with circuit

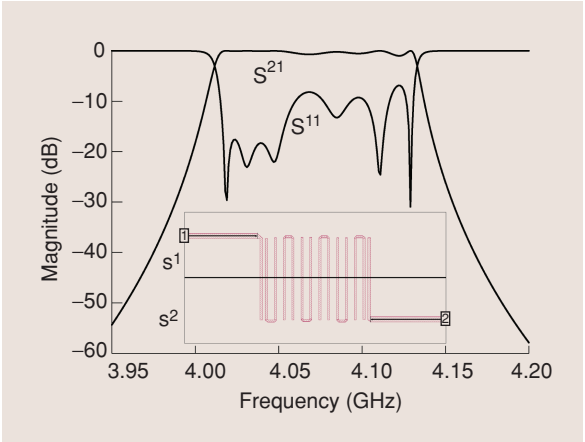

Figure 2. *Divide and conquer, or topological partitioning, applied to a filter. Split, as indicated, in half, each half EM analyzed and connected back together using circuit theory yields results exactly identical to the EM analysis of the complete filter (from [9]).*

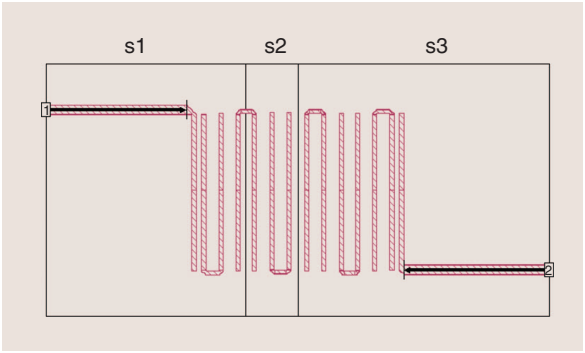

Figure 3. *Partitioning a filter between coupled resonators results in failure of the topological partitioning because coupling between partitioned sections is not included. Partitioning between the legs of a hairpin resonator might result in decreased accuracy because coupling between the legs is not included.*

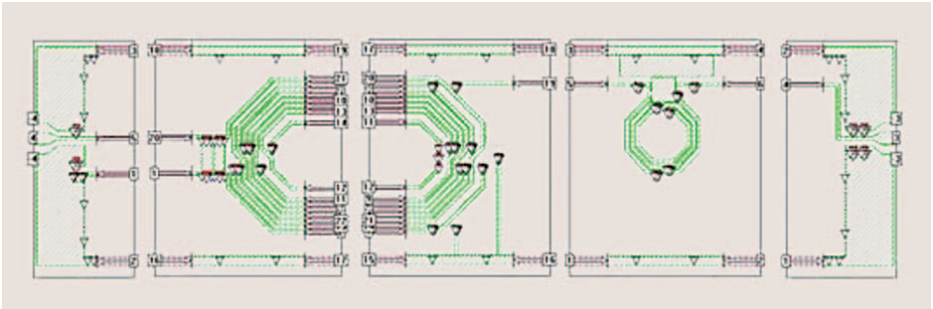

Figure 4. *A circuit on silicon from NXP is partitioned into five small circuits. Each small circuit is EM analyzed and connected back together using circuit theory yielding results almost identical an EM analysis of the complete circuit (from [12]).*

theory, do one more EM analysis to confirm the changes, then fabricate. Design closure, quick and easy: a *tunable* EM analysis!

Functional Partitioning

Sometimes we do not want a dividing line to go across the entire width of our circuit. For example, we cannot analyze an entire amplifier and its transistor all in one EM analysis. In fact, because it has a very fine geometry and it is nonlinear, too, we don't want to include the transistor in the EM analysis at all. If we use topological partitioning, we divide the amplifier into two halves: the input and the output circuits. Then we analyze each half and connect them back together, along with the transistor, using circuit theory.

This approach does not include the EM fringing fields that couple the output circuit back to the input circuit, which is important if you want to make an amplifier instead of an oscillator. Even with approximate port calibration, we can analyze the entire amplifier layout and include a pair of internal ports for the transistor. This actually works provided the frequency and power level is not too high. This limitation is removed with perfect port calibration.

For a first example, we use the same circuit as in Figure 4, only now partitioned functionally (Figure 5), also from [12]. The layout is separated into the CPW frame, a filter, and a balun. The frame uses internal ports with a floating ground reference. This is necessary in silicon because there is no global ground available for internal ports. Internal ports must be referenced to a floating ground. Fortunately, the internal port calibration algorithm is just as perfect using a floating ground reference as it is using a global ground reference. It is important, however, to remember that we can make connections (with our favorite circuit theory program) only between ports that have exactly the same ground reference. There are some exceptions that the advanced user can use, but a full explanation would be a little too much detail just now. In Figure 5, all ports connected to the same black box are calibrated to the same (floating) ground reference. Thus, we can use circuit theory to connect the balun and the filter functional portions into the CPW frame with no problem. Results are available in [12]; full EM analysis and functional partitioning yield nearly identical results over the entire range up to 10 GHz.

In the past, microwave designers have always used S-parameter data where all ports are referenced to the same global ground. When using functional partitioning in Si RFIC, it is required that the internal ports be normalized to a floating ground. (It is amazing that Si RFIC work has gotten as far as it has without the explicit concept of a floating ground reference.) We suggest that you do not directly view such S-parameter

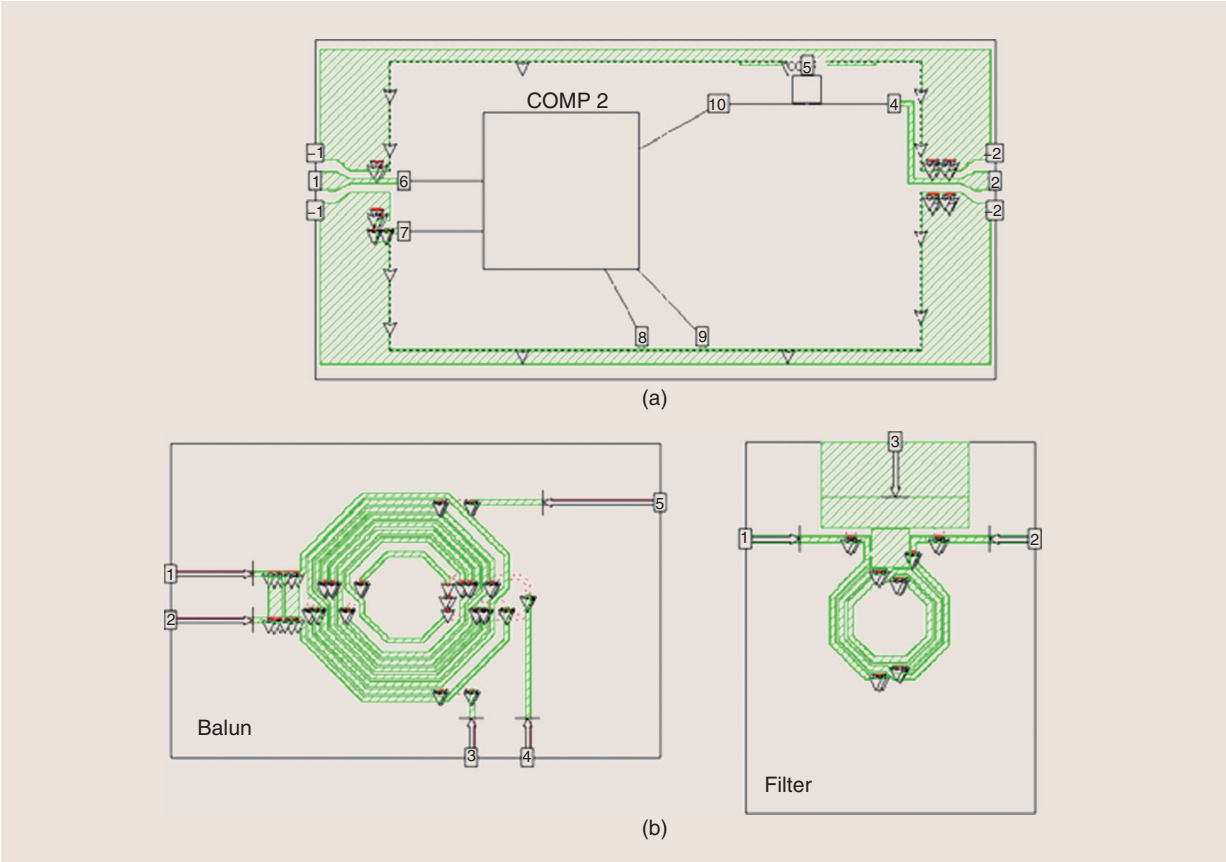

Figure 5. *Functional partitioning separates (a) a circuit based on function with internal ports added for (b) each component that is analyzed separately (from [12]).*

data, at least at first. It can appear very strange, depending on where the various ground references are floating. When you connect all the functional components into the circuit, things look normal.

A very important note for Si RFIC designers: When present, the CPW frame (or cage) can have a substantial effect on the circuit. Just because we call it ground does not mean it can be arbitrarily included or left out. If a functional block is analyzed or measured with a ground cage in place, then it must use that same ground cage in the circuit. If the layout of Figure 5 is used in a larger circuit, only without the CPW frame, entirely different results can be expected.

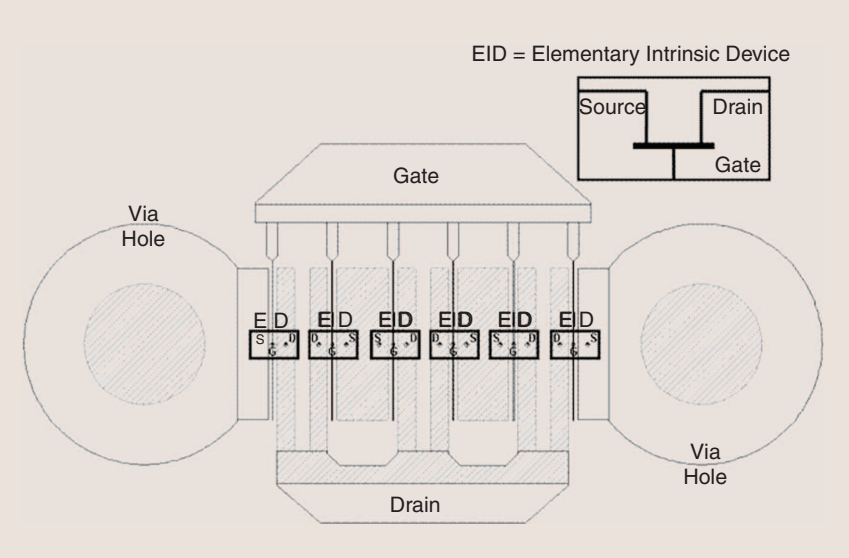

Figure 6. *Functional partitioning applied to a power FET allows the passive parasitics of the FET to be evaluated by EM analysis with internal ports on each FET finger allowing connection of the nonlinear sources and bias-dependent passives. This model is easily scaled (from [13]).*

Figure 6, from [13], is an example of functional partitioning on an entirely different scale. Here we are using functional partitioning *inside* a power FET. The passive, planar portion of the FET is analyzed in an EM analysis. Next, perfectly calibrated internal ports are placed in the middle of each FET finger for connection to the source, gate, and drain of each finger. Then an active model, the elementary intrinsic device (EID), is connected to each set of internal ports. The EID contains the active (including nonlinear) controlled sources and any bias-dependent passive models. The EM analysis provides all the passive parasitics of the entire device, including grounding vias. Figure 7 shows representative measured versus calculated over 4 to 65 GHz. As an added benefit, this model is easily modified by adding or subtracting FET fingers and by changing the gate width, yielding a scalable power FET model.

When using functional partitioning, one can remove all components from a complete design. This includes all active devices; resistors, capacitors, and even, at least in the case shown above, inductors. Next, put in place internal ports in the EM analysis at the location of each removed component. EM analyze the interconnect, including all component ports. Then, use your favorite circuit theory tool to connect models (lumped, S-parameter, vendor provided, EM generated, etc.) for each component back into the EM analyzed interconnect. Keep changing components (manually, or under automatic circuit theory driven optimization) until your circuit meets requirements. If the interconnect has been modified, repeat the EM analysis of the new interconnect and continue until your circuit meets requirements. Several more examples are described in [9] and [10]. Once more, we have created a *tunable* EM analysis!

This approach does not include fringing field coupling between components. If two components are very close and have significant coupling, then the two components should be treated as a single component.

Functional partitioning also solves what we call the *big-small problem*. This problem is seen in all EM analyses. One portion of a layout requires really fine meshing for extremely tiny geometries. Another portion is very large, but coarse meshing is acceptable. Simply make the fine portion (for example, a transistor) of the layout a separate component and proceed as above. The fine geometry is analyzed separately from the large

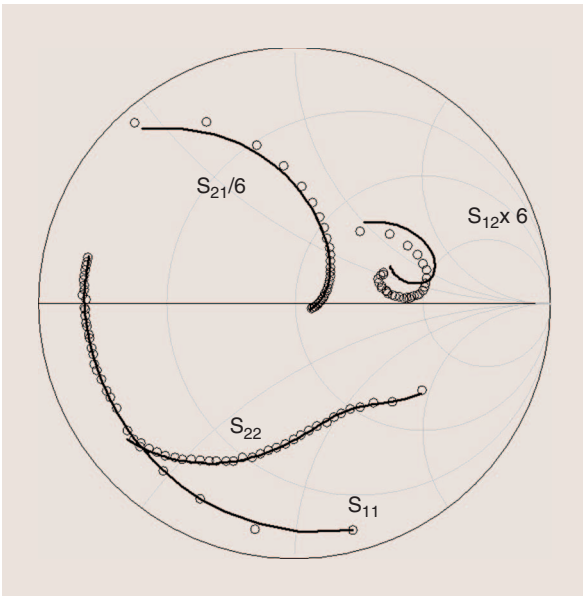

Figure 7. *Representative measured versus calculated of the functional partitioning in Figure 6 (from [13]).*

geometry (perhaps even using a different EM tool) and each with an optimal mesh size. The two are connected back together after the EM analyses are done.

Tuning Methodology

The tuning methodology is the most powerful technique for design closure; however, it requires not only knowledge of how the circuit works but also a certain degree of intelligence with respect to how to tune the circuit.

In my teenage days as a ham radio operator, circuits would have trim pots (screwdriver adjust variable resistors) and trim caps (small variable capacitors), among other tunable elements. To get the desired performance from a filter, amplifier, or an intermediate frequency (IF) strip, I would sit there using my tuning tool until I was satisfied. The tuning methodology is just an EM-analysis-based version of that process. The main problem is how to put the equivalent of trim pots, trim caps, etc., into the EM analysis. We do not want to do a complete EM analysis each time we change the value of one component slightly.

Figure 8 shows an eight resonator narrow-band filter from Dielectric Laboratories. Normal design time for a filter of this complexity is one to two weeks, assuming that success is realized on the first fabrication. Total manufacturing tolerance is under 0.5%, and that tolerance demands almost the entire error budget. There is little room left for design and EM analysis error. If we had, for example, another 0.5% of EM analysis error, we risk missing the filter requirements by up to a factor of two, requiring a second fabrication.

The right-hand inset in Figure 8 illustrates the insertion of tuning ports that allow modification of the input coupling section. Note that the ground symbol on each of the four added ports indicates all four ports are referenced to a global ground. If the global ground is far from the circuit, for example, with silicon, then floating ground ports would be used and no ground symbol would appear on the tuning ports. The tuning ports shown here are to illustrate the concept. In practice, a minimum distance gap between the ports (making them hard to see at this scale) might be used and there would be a set of tuning ports in every coupled line section of the filter and between every pair of end gaps (making the figure very complicated).

To implement the tuning methodology, insert a set of four ports in the center of each coupled line section, adding 16 ports to the circuit. Then insert a pair of perfectly calibrated ports in each gap between resonators, adding ten ports, for a total of 28 ports. Now, using circuit theory, connect an appropriate circuit theory coupled line between the coupled ports. You can tune the length of each coupled line section by tuning the length of the inserted circuit theory coupled line. You can add a capacitor between the lines (or an open circuited stub in parallel with the odd mode of the coupled lines) to adjust the coupling. For the five pairs of tuning ports between the resonator ends, add a circuit theory microstrip gap model plus a short length of microstrip line. Tune the gap width to adjust the resonator-to-resonator coupling. Tune the short length of microstrip line to adjust the length of each resonator. This can be done manually or under control of an automated circuit optimization program.

Using this technique shrinks the design time from several weeks down to one day or so. When a modified design is desired, a previous design can be tuned up to the new requirements in a matter of minutes to hours.

Figure 9 shows measured versus EM calculated results. Neither the filter nor the EM analysis geometry was tuned after fabrication; this result is a typical first-time turn-on result. Note that one should *never* tune dielectric constant, thickness, or loss in the EM analysis to anything different from what is independently measured. Such tuning can easily mask common measurement errors, thus inserting the measurement error into the EM analysis [14].

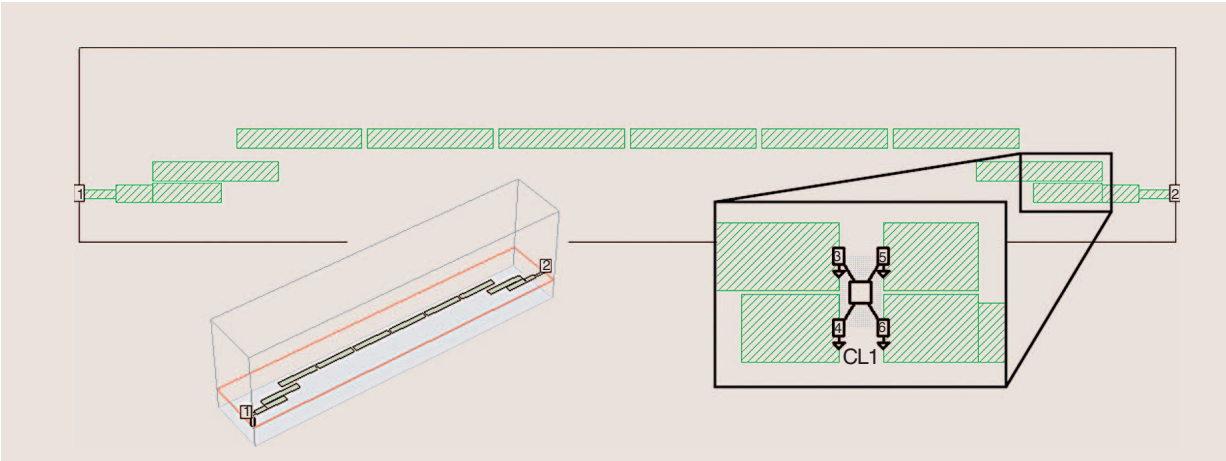

Figure 8. *Bandpass filter from Dielectric Laboratories illustrating the principle of tuning ports (in the inset at right) for the output section of the filter. When a full set of tuning ports are in place, filter tuning and modifications proceed at circuit theory speed.*

There are two EM analysis curves in Figure 9. The ceramic used by Dielectric Laboratories for this filter has almost exactly zero temperature coefficient over a wide range. However, the ceramic grains are not spherical and are oriented in a vertical direction. Thus, the ceramic has a degree of uniaxial anisotropy. The isotropic curve indicates results of an EM analysis using an isotropic dielectric constant tuned to yield the correct center frequency. Notice that this leaves the bandwidth substantially in error, a problem that would require multiple fabrications. Thus, while tuning ports enable a much faster design cycle, inclusion of anisotropy in this filter is critical to success on the first fabrication. A wide variety of substrates are anisotropic including all composite substrates that contain a woven fabric; for example, FR-4 and many Teflon-based substrates. Loss tangent can vary as much as a factor of two depending on E-field direction. As in Figure 9, tuning the EM analysis dielectric constant to some kind of average of the anisotropic dielectric constants can yield unacceptable results.

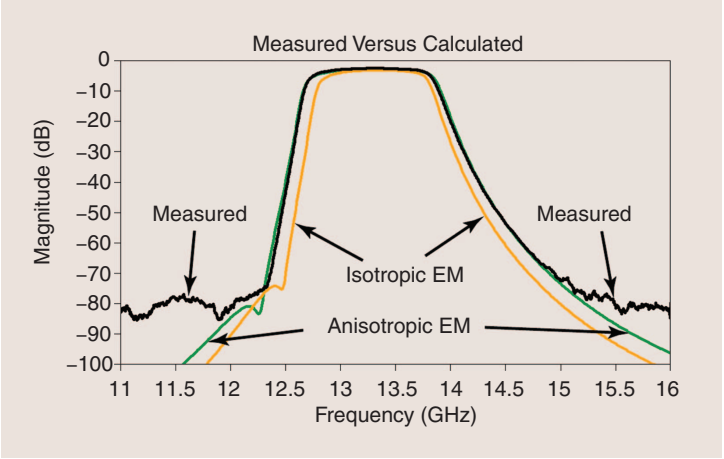

Figure 9. *Typical measured versus calculated for the filter of Figure 8 indicates that including the anisotropy of the substrate in the EM analysis is critical for success on first fabrication. The "isotropic" analysis uses a dielectric constant "tuned" to give the correct center frequency, yielding unacceptable results.*

Broadband Lumped Model Extraction

An increasing number of RF designers need to analyze their circuits in SPICE. This means a lumped (RLC) model is needed. It is important that the model be both stable and passive. One approach to extracting a lumped model is to find a pole-zero constellation that yields the same frequency response as the circuit. Then an RLC circuit is selected that corresponds to the same poles and zeros. The problem is that the circuit that results can be nonpassive and unstable, especially for complex circuits with many ports. This appears to be a widespread problem, even though there is little mention of it in the literature. A clue that this problem exists is that there has been substantial research effort reported with hopes of solving the problem. These reported solutions attempt to enforce passivity and stability when extracting a lumped model.

In our broadband lumped model extraction, we have seen unstable and nonpassive results. However, to date, all such problems are solved by taking more data and/or extracting more poles and zeros. It is our speculation that the reasons we have not seen unresolvable problems is because of our use of perfect port calibration. For example, the very small, but nonphysical, error introduced by approximate port calibration and Green's function calculation might easily throw poles into unstable regions at high frequency. In this case, an accurate lumped model extraction must return an unstable model because the data presented to the extraction corresponds to an unstable system.

So, rather than enforcing stability and passivity, perfect port calibration allows extraction of a naturally passive and stable lumped model. Examples are presented in [12] and [15].

Compact Model Synthesis

Model extraction starts with an assumed form for the desired model. In the case of broadband SPICE extraction described above, the model can grow to a required level of complexity; however, the underlying topology is fixed. In other cases, the designer selects a model based on experience and intuition and uses various creative means to find values for the elements of the model that yield a response similar to the EM analyzed (or measured) data.

Model synthesis, on the other hand, independently determines the best topology for the model. The only input to a synthesis is the S-parameter data for which a model is to be synthesized. The designer does not suggest a form for the model nor is any information about the specific component being modeled provided.

A compact RLC model synthesis was recently described [16]. The technique uses closed-form solutions to evaluate numerous potential RLC topologies based on data from up to five frequencies. Then, data from other frequencies are used to evaluate the degree of fit for each result. The best fitting model is then provided to the designer. If an appropriate lumped model exists in the synthesis solution space, then it is usually physical. You can look at the model schematic and realize what kind of component it is. Currently, the solution space for a two-port is well over 5×10^8 possible topologies. Typical synthesis times range up to a few seconds. For this, and many other model tasks, extreme EM accuracy is a big advantage (see the "Perfect Calibration Is Like a Hydrogen Car" sidebar).

Figure 10 shows a pair of coupled inductors on silicon from [12]. The set of all possible models for this

Perfect Calibration Is Like a Hydrogen Car

"While you can do EM simulations without perfect de-embedding, any residues left from the de-embedding remain in your model," observes one experienced microwave model developer. "Even tiny residues can cause huge problems in delicate modeling situations."

This modeler suggests performing the following test: In your EM software, de-embed a through line to zero length. Reflection S-parameter magnitudes should all be at the noise floor of the EM analysis (which should be well below 100 dB down) and transmission phase should be exactly zero degrees. Another test is to insert two internal ports with global ground reference in the through line (see Figure S1) with the external port reference planes set at the location of their mating internal ports. Now S_{34} magnitude (as well as all reflection magnitudes) should be at the noise floor. These tests are most sensitive to error when the through line is long and the substrate is thick and lossy. For both internal and external ports, it is wise to check multiple ports at small and large separations by using multiple coupled through lines.

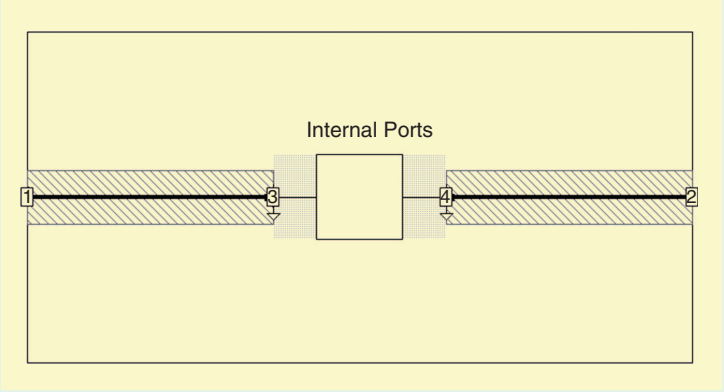

Figure S1. *A simple circuit provides an acid test for internal ports. When there are hundreds of internal ports, even small port calibration error is magnified.*

Based on his extensive experience, our modeler leaves us with this evocative image, "When I think of EM analysis results that use approximate port calibration I get this messy image of an engine not cleanly burning its fuel and leaving sticky deposits behind. Perfect port calibration is like a hydrogen car, leaving exhaust that is perfectly clean."

inductor with error under a certain threshold was prepared for a range of separations (the gap between the two spirals). The lowest error model topology present for all values of separation was then synthesized for all values of separation. The values for the RLCs for each value of separation were fitted by means of regression. Most element values require only a linear ($y = ax + b$) fit with some requiring as much as a cubic spline.

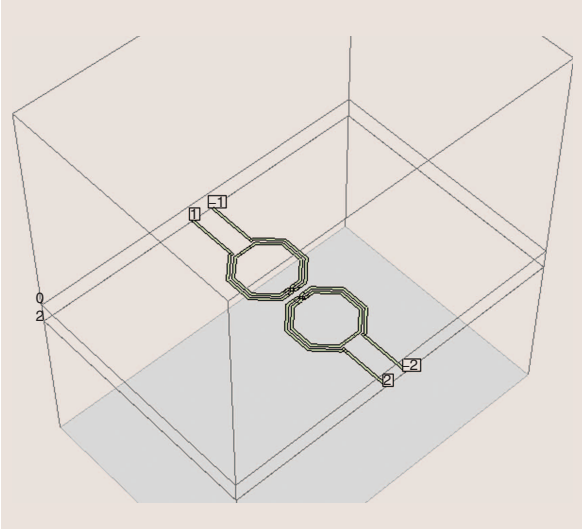

Figure 10. *Two mutually coupled spiral inductors on silicon are modeled as a function of their separation (the gap between the two inductors), after [12].*

The result is a parameterized model of the mutual coupled inductors (Figure 11). The model was implemented in AWR Microwave Office. Figure 11 shows the EM analysis at the two limits of separation and the model with the separation parameter midway between. This model is valid up to 20 to 30 GHz. Reflection coefficient (not shown) for this model is in error by up to 0.1 dB or so. If we limit the desired validity of the model to 10 GHz, the synthesized model yields essentially exact agreement. Full details on this model will be published later.

This model does not use a mutual inductance (symbol K in SPICE). Mutually coupled inductors can be modeled as either a T network or as a π network [16]. Either model works well for this case, with the π model working slightly better. Note that a large inductance connected between Ports 1 and 2 indicates small inductive coupling. In this case, π mutual inductors with values of a few hundred nH are synthesized. The SPICE mutual inductor, K, is not appropriate for use on silicon because it does not include loss. In silicon, loss is an important factor for mutual inductance.

We can easily reverse one of the ports in Figure 10. For example, make one negative numbered port positive, and make the mating positive numbered port negative. In this case the lumped network connecting Ports 1 and 2 becomes all negative-valued elements. This model is still stable and passive. It simply means that positive current on the signal (positive numbered) terminal of Port 1 creates positive current on the signal terminal of Port 2. The way we normally connect circuits, positive current

on Port 1 (i.e., current going into Port 1) generates negative current on Port 2 (i.e., current going out of Port 2). With the ground references of Ports 1 and 2 isolated, this is no problem for circuit theory and is actually common. This is an illustration of the fact that restricting lumped models to all positive elements makes it impossible to model certain components [16].

This inductor does not include a CPW frame/ground cage. The isolation between the two inductors is substantially changed if such a frame is included [12].

Artificial Neural Net Models

Another modeling approach is built around artificial neural networks (ANNs). This technique learns how to model a system as a function of various user-selected parameters based on results for a set of values of those parameters. For example, the coupled spiral inductors above could have also been modeled by means of a neural network. In contrast to the previous approach, a neural network does not give physical insight into the system being modeled. On the other hand, it is completely general. A good overview is [17].

In [18], Sonnet provides data at adaptively and automatically selected points in the parameter space to train a neural network to user specified accuracy. In [19], a neural network adjusts the RLC values in a lumped equivalent circuit as well as the coefficients in a state-space representation of components embedded in an overall circuit. The component values and equation coefficients are adjusted to move the components to different points in the parameter space (i.e., for different component sizes and shapes) so that optimization can proceed quickly. This approach additionally allows time-domain analysis. The neural network is trained by automatically launching a minimum set of required EM analyses. Most recently, a technique that finds a global optimum in the presence of multiple local minima for neural network training has been reported [20].

Another excellent overview is [21]. Substantial applied neural network modeling is reported in [22] in a detailed scalable power FET model. Freescale Semiconductor Inc. has demonstrated the applicability of this technique on wide ranges of device technologies for passive microwave components including open end, step, tee, planar inductor, capacitor, etc. Very high EM accuracy, especially with regard to perfect port calibration, has been found to be critical in this modeling effort.

Neural networks are used in [23] (Figure 12) to design and optimize a complete transmitter, including the transmitter's interaction with its antenna. Because of the

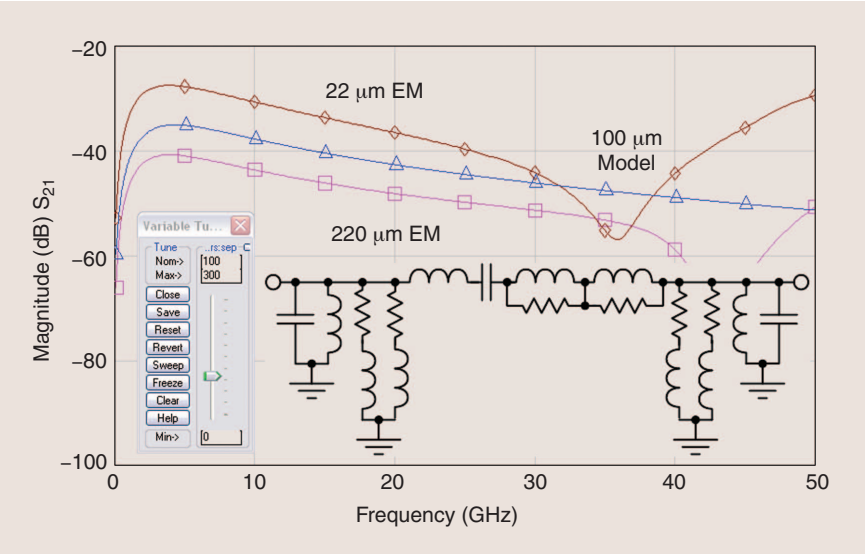

Figure 11. *The synthesized lumped model for the coupled inductors of Figure 10. Each RLC is a simple function (linear up to cubic) of the inductor separation. The model is evaluated for an inductor separation of 100 μm, midway between the EM results shown for 22 μm and 220 μm separation; after [12].*

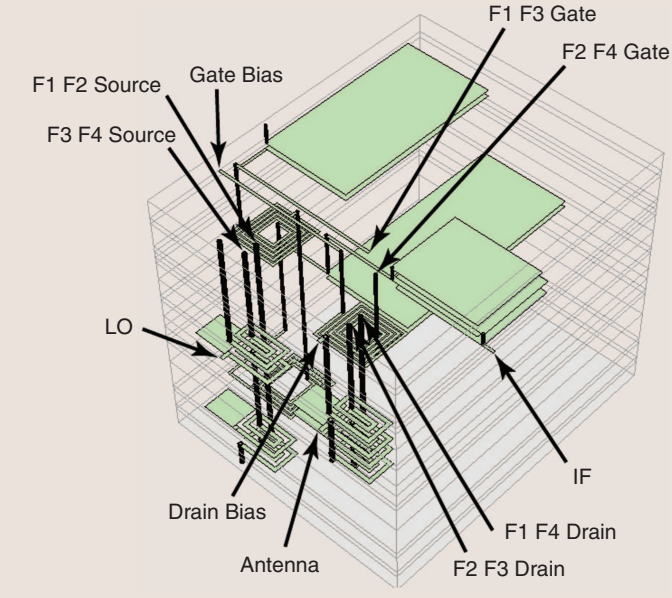

Figure 12. *The transmitter portion of a module analyzed with EM analysis based topological partitioning driving artificial neural network model generation. The complete circuit includes a 3-D aspect requiring use of multiple EM tools.*

antenna, a portion of the circuit involves a 3-D arbitrary aspect, more appropriate for a volume meshing tool. This is an excellent example of a project requiring multiple EM tools as both Sonnet (a planar surface meshing frequency-domain tool) and CST Microwave Studio (a volume meshing time-domain tool) were used. This also illustrates why software-vendor-supported interoperability between tools is especially useful. In this case, both EM tools train multiple neural network models, including a separate neural network for each frequency required by the nonlinear harmonic balance analysis used in the work. The analysis uses topological partitioning and requires 11 ports (Figure 12). If functional partitioning and tuning methodology were to be used in addition, even more ports would be required. Large numbers of precisely calibrated internal EM analysis ports are typical of new designs.

Preceding and inspiring widespread work in ANN research, the application of space mapping [24] to microwave design has also seen substantial research and development. Space mapping is a group of related techniques that minimize the number of time-consuming EM analyses (fine model) by substituting a fast coarse model for most of the optimization work. It is possible that the new design methodologies described above can be cast into the framework of space mapping. Illustrating the flexibility of space mapping, it has been recently adapted to take advantage of perfectly calibrated internal ports [25] in a manner similar to the tuning methodology. Space mapping promises to see significant advantage as we learn how to combine it with perfectly calibrated internal ports.

Conclusions

For the last 25 years, as EM analysis has gradually penetrated the microwave design cycle, it has been sufficient to settle for a good enough level of accuracy. In other words, the measured and calculated curves on a plot are reasonably close. Over the last several years, a new approach to microwave design has been taking hold. Specifically, the EM analysis now includes numerous (dozens, even hundreds) additional ports, for which extreme accuracy in port calibration is both required and is now available. These extra ports allow a designer to achieve design closure at circuit theory speed, but with EM accuracy. Several forms for this new design cycle, including topological partitioning, functional partitioning, and tuning methodology, are described. This extreme port calibration accuracy also has substantial impact on various model extraction and synthesis techniques. All of these techniques are now being vigorously and successfully developed in applied situations with new developments and refinements being seen on almost a daily basis. Wide application is expected over the next several years.

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