

### C. The Problematics of the Variational Formulation

It would be tempting to use the variational formulation for TE modes which consist of using the boundary condition  $\partial\psi/\partial n(\mathbf{r}) = 0$ ;  $\mathbf{r} \in l$ , as the eigenvalue equation. We obtain a symmetric equation with respect to  $\mathbf{r}$  and  $\mathbf{r}_o$ :

$$-\int_l \frac{\partial^2 G_k(\mathbf{r}, \mathbf{r}_o)}{\partial n \partial n_o} \psi(\mathbf{r}_o) dl_o = 0. \quad (\text{A9})$$

This formulation cannot be correct since, as pointed out in [4], the normal derivative of  $\psi$  at  $l$  has a delta function. This is due to the fact that  $\psi$  has an extremum over  $l$  and vanishes outside  $S$ . If we define an eigenvalue equation from (A9) its elements will not converge with respect to  $m$  and  $n$  in the Green's function. The existence of the delta function and its influence on  $\psi$  can be verified numerically. We take for example the first TE mode for a rectangular waveguide. The cutoff wavenumber and  $\psi(\mathbf{r}_o)$  are known analytically and can be inserted into the expression for  $\partial\psi/\partial n$  and then calculated.

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## Synthesis of Lumped Models from $N$ -Port Scattering Parameter Data

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**Abstract**—A closed form technique is described which allows the synthesis of an  $N$ -node lumped network from  $N$ -port scattering parameter ( $S$ -parameter) data. The synthesis is appropriate for networks where  $N$  is very large, for example, high speed digital interconnect networks. The resulting lumped model can be used in SPICE and other simulators. The synthesis is valid for any structure that is small with respect to wavelength. Thus it is also appropriate for synthesizing lumped models of simple discontinuities, such as step junctions and cross junctions. A description of the theory and several examples are provided.

### I. INTRODUCTION

When a lumped model of a structure (e.g., discontinuity) is desired, one approach is to first obtain  $S$ -parameter data. This data can be obtained by measurement or by numerical calculation. Then, a trial lumped model is selected based upon the designer's experience. The model is evaluated by adjusting the values (usually by means of an automatic optimizer) of the elements so that the resulting  $S$ -parameters match, as closely as possible, the measured (or calculated) data. If it is not possible to achieve a match to the desired accuracy, the model is deemed inappropriate and another model is evaluated.

This procedure can be time consuming and frustrating. In addition, the resulting model may be more complex than is needed. With this in mind, a synthesis technique was developed. The synthesis technique starts with the  $S$ -parameters, at two frequencies, of the structure of interest. It then synthesizes a lumped model using closed form equations. When provided with  $N$ -port data, the synthesis results in an  $N$ -node lumped model ( $N + 1$  nodes, if ground is counted), where each node corresponds to a port in the original data. The lumped model allows for all possible connections of lumped elements between nodes.

With the exception of a series resistor-inductor, internal nodes are not allowed. Thus an LC ladder network between ports is not allowed. For this reason, the electrical distance between any two connected ports must be small compared to the shortest wavelength of interest. This is easily checked for a specific circuit by simply synthesizing a model at two different pairs of frequencies. If the models do not agree with each other to the desired degree, then this assumption is violated at least at the highest frequency used in the synthesis.

In fact, synthesizing successive models over an increasing range of frequencies is an excellent way to check the validity of a model. The frequency at which the lumped model starts to change is the model's limit of validity. In this situation, one may place more ports in the circuit. The ports may be internal, or the structure may be sub-divided into smaller structures. This results in a more complex model, as is required to increase the range of validity for a lumped model.

In the microwave field, this technique is useful in synthesizing lumped models of discontinuities. Examples include step, tee, and cross junctions, overlay capacitors, and FET (field effect transistor) manifolds.

Since the technique is appropriate for very large  $N$ , lumped models of entire high speed digital interconnect networks may also be synthesized. For large  $N$ , calculated data is the most appropriate

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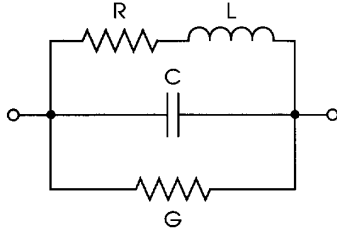


Fig. 1. This lumped circuit is used to provide an arbitrary connection between nodes.

target for synthesis since making all the required measurements becomes difficult.

This technique was developed in September 1991 and has been available in commercial software since December 1991 [1].

## II. THEORY

The technique allows the RLCG circuit of Fig. 1 to be connected, as needed, between pairs of nodes, forming the lumped model. Each port of the circuit, in addition to ground, can be a node. If we are given, at two frequencies, the numerical values of the admittance between two nodes, we may solve for the values of  $R$ ,  $L$ ,  $C$ , and  $G$  to be connected between those two nodes. The admittance of the lumped model of Fig. 1 is

$$Y = G + j\omega C + \frac{R - j\omega L}{R^2 + \omega^2 L^2} = \left( G + \frac{\frac{1}{R}}{1 + \frac{\omega^2 L^2}{R^2}} \right) + j \left( \omega C - \frac{\frac{\omega L}{R^2}}{1 + \frac{\omega^2 L^2}{R^2}} \right). \quad (1)$$

Next, we make the assumption that  $R \ll \omega L$ , as discussed later. We now have

$$Y = \left( G + \frac{R}{L} \omega^{-2} \right) + j \left( \omega C - \frac{1}{L} \omega^{-1} \right). \quad (2)$$

Now, the imaginary part of the admittance is a linear equation in the two unknowns,  $C$  and  $1/L$ . Given measurements (or numerical calculations) of the actual admittance ( $g_0 + jb_0$ , and  $g_1 + jb_1$ ) at two distinct frequencies ( $\omega_0$ , and  $\omega_1$ ), we have a system of two linear equations in two unknowns, the solution of which is

$$L = - \frac{\frac{\omega_0}{b_1 \omega_0 - b_0 \omega_1} - \frac{\omega_1}{b_0 \omega_0 - b_1 \omega_1}}{b_1 \omega_0 - b_0 \omega_1} \quad (3)$$

$$C = \frac{b_0 \omega_0 - b_1 \omega_1}{\omega_0^2 - \omega_1^2}. \quad (4)$$

Using the solution for  $L$  and  $C$ , the real part of (2) also becomes a linear equation in two unknowns,  $G$  and  $R$  with the solutions

$$R = L^2 \frac{g_1 - g_0}{\omega_1^{-2} - \omega_0^{-2}} \quad (5)$$

$$G = \frac{g_0 \omega_0^2 - g_1 \omega_1^2}{\omega_0^2 - \omega_1^2}. \quad (6)$$

Equations (3)–(6) specify the values of the lumped elements to be connected between the two nodes.

Given the  $N$ -port  $S$ -parameters, the admittance to be used in the above equations may be determined by converting the  $S$ -parameters to  $Y$ -parameters. The admittance to ground of the  $i$ th node (port) is given by the sum of the  $i$ th row (or column). The admittance connecting the  $i$ th and  $j$ th nodes is the value of  $Y_{ij}$ .

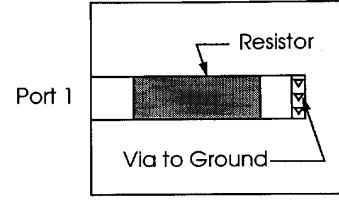


Fig. 2. A resistor (shaded area) 1 mm by 3 mm is grounded with a via 1 mm from the end of the resistor. The resistor is 1 Ohm per square for a total resistance of 3 Ohms. The substrate is GaAs 1 mm thick. The subsection size is 0.25 mm and the electromagnetic analysis required less than one second per frequency for analysis on an HP 710.

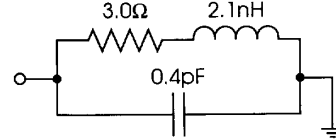


Fig. 3. The lumped model synthesized from the electromagnetic analysis of the resistor of Fig. 2. The values were derived directly from the  $S$ -parameters of the resistor at 3 and 3.1 GHz.

We still need to justify the assumption that  $R \ll \omega L$ . Consider what happens if the assumption is violated. If in fact,  $R \gg \omega L$ , then the real part of  $Y$  (2) is frequency independent and the numerator of (5) is zero, resulting in  $R$  equal to zero. However, the model is still valid, because a frequency independent real part of  $Y$  is properly modeled by  $G$ , (6). So, when the assumption  $R \ll \omega L$  is violated, the required resistance in the network simply transfers from  $R$  (5) to  $G$  (6). The resulting model is still valid.

Although not described here, extraction of mutual inductance from the data is also possible if desired. When mutual inductance is included in the model, the model (and synthesis frequencies) become equivalent to the  $S$ -parameter data. When you have one, the other is determined.

## III. EXAMPLES

In the examples that follow, electromagnetic numerical analysis [2], [3] is used to provide the initial  $S$ -parameter data. The data could also have been provided by any other numerical analysis or by direct measurement.

In the first example, we explore the implications of the assumption  $R \ll \omega L$ . As shown in Fig. 2, we investigate a resistor with aspect ratio of 3:1 and a surface resistance of 1 Ohm per square (a 3 Ohm resistor). At 1 MHz, the calculated reflection coefficient is 0.887692 at 179.97 degrees. At 2 MHz, we have 0.886792 at 179.94 degrees. The resulting synthesized model is a 3.0 Ohm resistor to ground.

Evaluating the same circuit at 3 GHz and 3.1 GHz, we obtain 0.886323 at 80.25 degrees and 0.887099 at 76.51 degrees, resulting in the lumped model of Fig. 3. From this data, it is easily verified that  $R \ll \omega L$  at 3 GHz and that the reverse is true at 1 MHz.

When 4 GHz and 4.1 GHz are selected as synthesis frequencies,  $R$  decreases to 2.6 Ohms, suggesting that the upper limit of validity for a lumped model of this complexity for this structure is between 3 and 4 GHz. The electrical length of the structure is about 60 degrees at 3 GHz.

Fig. 4 shows a more complex circuit. This is a power FET gate manifold on 100  $\mu\text{M}$  GaAs. The input line is 70  $\mu\text{M}$  wide and each FET gate attachment point is 10  $\mu\text{M}$  wide. The actual gate dimension (after attachment) is not important for this model synthesis. For this

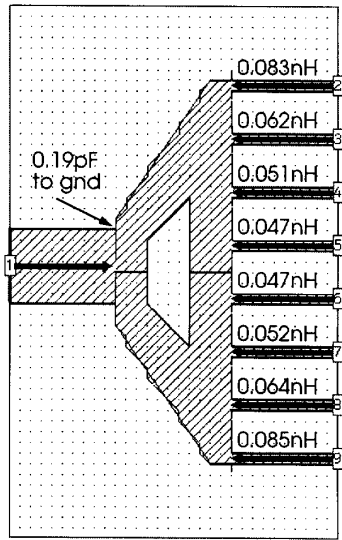


Fig. 4. The power FET gate manifold splits power input from port 1 to each gate port. The hole in the center forces more equal phase distribution. Analysis time was about 30 seconds per frequency with a 10  $\mu$ M cell size. Triangle subsections were included to smooth the diagonal edges. The  $S$ -parameter data was de-embedded to the reference planes indicated by the arrows. Values obtained for the lumped model inductors from port 1 to each gate port are indicated.

gate manifold design, a hole is placed in the center to force an equal phase distribution of the power fed to each gate across the width of the manifold. This allows increased FET efficiency and improved maximum power rating by changing only the manifold metallization.

The synthesis results include only one capacitor, from port 1 to ground, of 0.02 pF. All ports are connected by inductors. The inductors of interest are from port 1 to each gate port. Values are indicated in Fig. 4. The listed value of each gate line is the inductance from the tip of port 1 reference plane arrow to the tip of each gate reference plane arrow. The slight asymmetry in values is due to the slight asymmetry in the input port. Mutual inductors were also calculated.

Fig. 5 shows a high speed digital interconnect. It consists of 32 ports on the input (left side) and 32 ports on the output (right side). This is a two level circuit with a total of 64 ports. The metal on the second level is shown with dashed lines. Triangles pointing down indicate vias connecting down to the second level. This circuit requires 15 minutes per frequency on a SPARCstation II for the electromagnetic analysis. Once the  $S$ -parameter data is complete, lumped model synthesis is essentially instantaneous. With very loose limits (for example, including all capacitors greater than 0.005 pF), this structure results in an 1800 component lumped model.

Fig. 6 shows the result of the analysis of the cross-talk between two conductors as obtained with CONTEC SPICE. A 1.0 Volt pulse with a rise time of 10 pS was placed on port 1. The conductor connecting ports 25 and 57 has the strongest coupling. Fig. 6 shows the time domain response.

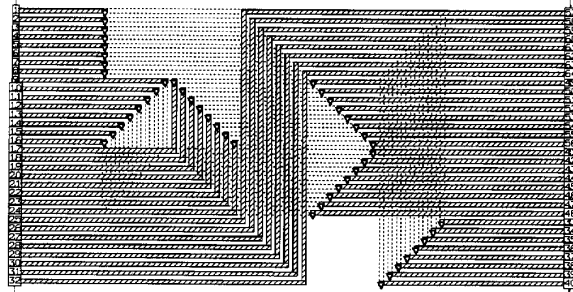


Fig. 5. The byte-reversal network for a 32 bit bus has 64 ports. For example, the high order 8 bits on input (upper left corner) come out as the low order 8 bits on output (lower right corner). The second level of metallization is shown with dashed lines.

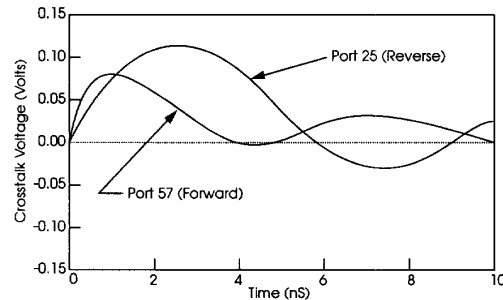


Fig. 6. With a 10 pS rise time, 1 volt pulse on port 1, the coupling to the port 25-57 line is shown. This is the result of a SPICE analysis of the model synthesized from the structure of Fig. 5.

IV. CONCLUSION

A new technique for synthesizing an  $N$ -node lumped model directly from  $S$ -parameter data has been described. The technique is valid as long as the structure being modeled is small compared to wavelength. In microwave application, discontinuities such as cross junctions, MIM capacitors, and others can be modeled. Since the synthesis is practical for large  $N$ , this technique is also appropriate for high speed digital interconnect modeling.

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