Unification of Double-Delay and SOC Electromagnetic Deembedding

James C. Rautio, *Fellow, IEEE,* and Vladimir I. Okhmatovski, *Member, IEEE*

***Abstract*—Double-delay and short open calibration (SOC) deembedding are both useful for deembedding the results of a gap voltage source excited electromagnetic analysis. Previously, each approach has been viewed as distinct, each with its own advantages and disadvantages. This paper describes a unifying theory, showing that double delay and SOC are each special cases of an extended SOC technique. Results related to the characteristic impedance as determined by this extended SOC deembedding are also presented.**

***Index Terms*—Calibration, characteristic impedance, deembedding, electromagnetic (EM) analysis, method of moments (MoM).**

I. Introduction

In an electromagnetic (EM) analysis, a circuit, or device-under-test (DUT), can be excited with "ports", often gap voltage sources. The circuit parameters (e.g., Y-, Z-, or S-parameters) are then determined from the voltage–current relationships seen at each port of the structure. For a frequency-domain analysis of an N-port, the circuit parameters are one $N \times N$ complex matrix at each frequency.

A discontinuity associated with the exciting port is necessarily included in the result. Electromagnetically, the port discontinuity is represented by fringing fields and transverse current flow (if any) in the vicinity of the gap voltage source (numbered in Fig. 1). From a circuit theory point-of-view, the port discontinuity takes the form of capacitances and inductances (Figs. 2 and 3). If there is loss, the port discontinuity also includes resistance.

The port discontinuity is usually small. For example, the shunt capacitance is typically on the order of a tenth of a picofarad. In some cases, the port discontinuity can be ignored. However, in many cases, it must be carefully evaluated and removed.

In addition, it may be desirable to shift the reference plane from the port to the interior of the circuit. In this case, the transmission line connecting the port to the circuit must be characterized and removed. In this process, the characteristic impedance (Z_0) and effective relative dielectric constant $(\varepsilon_{\text{eff}})$ of the line can be determined.

The double-delay deembedding performs this calibration by using EM analysis results of two through lines, a line of length L, and a second line of length $2L$ [1] [see Fig. 1(a) and (b)].

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J. C. Rautio is with Sonnet Software, North Syracuse, NY 13213 USA (e-mail: rautio@sonnetsoftware.com).

V. I. Okhmatovski is with the Department of Electrical and Computer Engineering, University of Manitoba, Winnipeg, MB, Canada R3T5V6 (e-mail: okhmatov@ee.umanitoba.ca).

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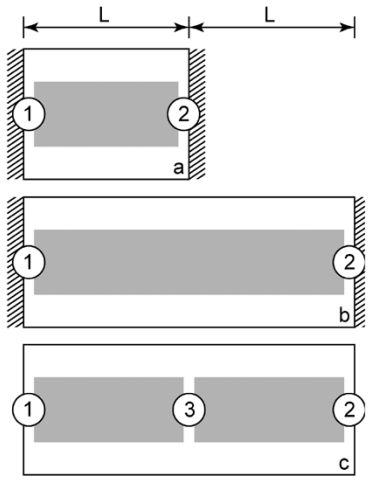

Fig. 1. Double-delay calibration uses: (a) an L-length and (b) a $2L$-length through line. The ports must be backed by a perfectly conducting electric wall. The SOC uses: (c) a single three-port $2L$-length standard. Perfect ground reference is not needed.

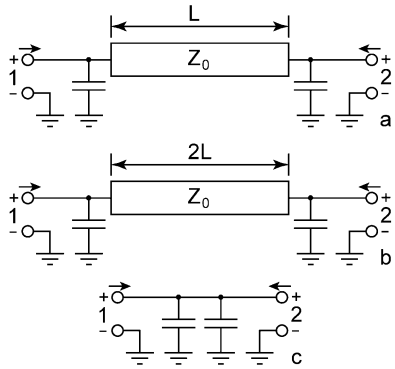

Fig. 2. Circuit theory model for the L and $2L$-length through of the double-delay calibration shows ports as a pure shunt admittance. After manipulating the cascading matrices, the double port discontinuity (c) remains.

The SOC calibration [2] uses a single through line of length $2L$, but there is a third port in the middle of the line, Fig. 1(c). The double-delay deembedding was generalized to multiple coupled ports in the original study [1] and the short-open-calibration (SOC) was generalized to multiple coupled ports in [3] and [4]. Some of the relative advantages and disadvantages are discussed in [5] and [6] and summarized here.

Double delay requires the port discontinuity to be a pure shunt admittance, no series impedance is allowed. A port discontinuity specialized in this way is easily realized in a shielded EM analysis. In contrast, the SOC characterizes arbitrary reciprocal port discontinuities. This is typical of port discontinuities seen in unshielded EM analysis. Thus, double delay can be used only in

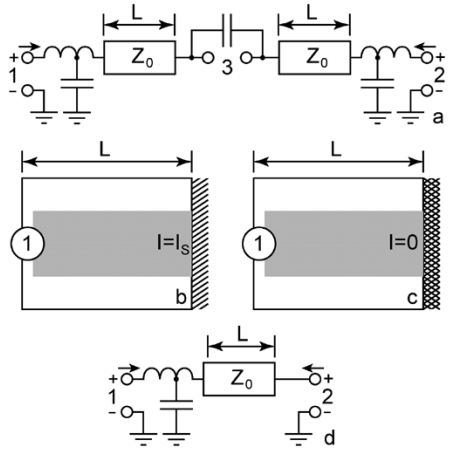

Fig. 3. Circuit theory model of the SOC standard: (a) includes arbitrary reciprocal port discontinuities. By exciting ports 1 and 2 symmetrically and antisymmetrically either: (b) an electric wall or (c) magnetic wall can be placed at the location of port 3. This allows characterization of a single-port discontinuity plus (d) connecting transmission line.

shielded analysis [7], [8]. SOC is typically used in unshielded analysis, but can, in principle, be used in either type of analysis.

Double delay has the advantage of characterizing the naked port discontinuity, i.e., the port discontinuity all by itself with no port-connecting transmission line. In addition, double delay also characterizes the port connecting line by itself (port discontinuities removed). The velocity of propagation and characteristic impedance of the port connecting line can then be inferred from the resulting circuit parameters.

The SOC characterizes the entire port discontinuity and port connecting transmission line together. Lacking a characterization of the port connecting line by itself, characteristic impedance and velocity of propagation are not determined. In addition, the entire port discontinuity plus connecting line is removed from the DUT, shifting the reference plane to a distance L from the port. Removal of the naked port discontinuity by itself, leaving the reference plane at the port, is not part of the SOC, as formulated in [2]. By additionally analyzing a DUT that is a length L of line (requiring the analysis of a $3L$ length of line in [9, Fig. 1]), an arbitrary naked port discontinuity can be characterized using the original SOC. The extended SOC, described in Section VI, achieves this same result by analyzing only an additional L-length line.

For double delay, the naked port discontinuity and the port connecting line are both characterized as separate entities. Thus, if only the naked port discontinuity is removed from the DUT data, the reference plane remains at the location of the port. If the port connecting line is also removed, the reference plane is moved into the DUT by length L.

In this paper, we briefly describe the double-delay and SOC theory and show how the calibration data sets from each technique are related. With this knowledge, we illustrate a faster means of obtaining the double-delay data set by using a SOC-like technique. We also describe an extension of the SOC theory using double-delay techniques that allows the SOC to characterize the naked port discontinuity and the connecting line separately. Both the original SOC and double delay are special cases of this extended SOC. We conclude with a discussion of characteristic impedance as determined by this extended SOC.

II. Double-Delay Theory Summary

Fig. 2 shows the circuit theory equivalent of the L- and $2L$-length double-delay calibration standards. The port discontinuities are illustrated with shunt capacitors to ground. First, obtain EM analysis results for both standards. Then convert the data to $ABCD$ cascading parameters. Invert the $ABCD$ matrix for the $2L$ standard and then pre- and post-multiply it by the $ABCD$-parameters of the L-length standard.

Inverting an $ABCD$ matrix converts all transmission lines to negative length and all lumped elements to negative values. For example, cascading a positive shunt capacitor with an identical, but negative shunt capacitor cancels both capacitors, leaving a perfect zero length through. Similarly, cascading a positive L-length line with a negative L-length line cancels both lines.

Following the above triple cascade (positive L-length line, negative $2L$-length line, positive L-length line, including port discontinuities), we have nothing left, except a double port discontinuity [see Fig. 2(c)]. If there is any series component in the port discontinuity, then the single port discontinuity cannot be determined from external measurements. However, if we assume the port discontinuity is a pure shunt admittance Y_C, the $ABCD$-parameters of the double-port discontinuity (indicated by subscript $2P$) are

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{2P} = \begin{bmatrix} 1 & 0 \\ 2Y_C & 1 \end{bmatrix}. \tag{1}$$

The single (naked) port discontinuity is obtained by dividing C (of the $ABCD$ matrix) by two.

This form of the single-port discontinuity yields an easy test of deembedding validity. If the pure shunt port discontinuity assumption is violated, or if any of several well-understood deembedding failure mechanisms are present [1], [5], [6] then A, B, and D differ from the indicated values. This self-diagnostic ability is critical in applied design where any analysis or design failure must be identified and corrected prior to fabrication. This self-diagnostic ability is not directly available in the original SOC, but is available in the extended SOC when applied to a shielded environment.

Now we deembed the L-length line by inverting the single-port discontinuity $ABCD$-parameters and pre- and post-multiplying the L-length line $ABCD$-parameters. The $ABCD$-parameters for an ideal TEM L-length line are

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\mathrm{TEM}} = \begin{bmatrix} \cos(\beta L) & jZ_0 \sin(\beta L) \\ j(1/Z_0)\sin(\beta L) & \cos(\beta L) \end{bmatrix}. \tag{2}$$

By equating the above expression for an ideal L-length TEM line to the numerical results for the deembedded L-length calibration through, one may solve for both βL (the electrical length) and the characteristic impedance Z_0. This is known as the TEM equivalent characteristic impedance [10]. Note that this impedance is not in any way determined based on transverse fields in the cross section of the transmission line.

Rather, this is the only characteristic impedance consistent with the current–voltage behavior at the terminals of the line.

The actual deembedding of the DUT is performed by inverting the naked port discontinuity $ABCD$ matrix and appropriately multiplying the DUT $ABCD$ matrix. If the reference plane is to be shifted, then the deembedded L-length line $ABCD$-parameters are inverted and used to appropriately multiply the DUT $ABCD$ matrix.

If multiple coupled lines and ports are involved, then all matrix elements in the above discussion become matrices themselves. This is the case for all deembedding schemes discussed in this paper. No other special consideration for multiple coupled ports is needed.

III. SOC Theory Summary

In SOC, the deembedding process includes the transmission lines extending by length L from the ports. The extended transmission lines separate excitation ports from the DUT and deliver quasi-TEM eigenmodes, uncontaminated by fringing fields, to the DUT. The SOC removes the contribution from the line extension L and the naked port discontinuity [see Fig. 3(d)] by evaluating the short and open standards shown in Fig. 3(b) and (c), respectively. The perfect L-length short and open terminations are evaluated through symmetric and antisymmetric excitation of a single $2L$-length SOC standard [see Figs. 1(c) and 3(a)]. The three-port $2L$ standard is characterized by a (3×3) Y-matrix typically evaluated using the method of moments (MoM)

$$[Y^S] = \begin{bmatrix} Y_{11}^S & Y_{12}^S & Y_{13}^S \\ Y_{21}^S & Y_{22}^S & Y_{23}^S \\ Y_{31}^S & Y_{32}^S & Y_{33}^S \end{bmatrix}. \tag{3}$$

SOC uses only data from the first two columns of (3). Physically, this means excitation voltage is applied only to ports 1 and 2. For all data used by SOC, port 3 is shorted, effectively removing the fringing capacitance [see Fig. 3(a)] across port 3. It is critical that the port-3 discontinuity have no series impedance. Using superscripts E for the (2×2) Y-matrix of the calibration standard terminated with a perfect electric conductor (PEC) [see Fig. 3(b)] and superscript M for perfect magnetic conductor (PMC) termination [see Fig. 3(c)], we have

$$Y_{11}^E = Y_{11}^S - Y_{12}^S \quad Y_{21}^E = Y_{31}^S - Y_{32}^S \quad Y_{11}^M = Y_{11}^S + Y_{12}^S. \tag{4}$$

These three Y-parameters, plus the condition of reciprocity $(ad - bc = 1)$, completely determine the SOC error box $ABCD$ matrix [2]–[4] corresponding to Fig. 3(d) as follows:

$$\begin{bmatrix} a & b \\ c & d \end{bmatrix} = \begin{bmatrix} Y_{21}^E \cdot \left(Y_{11}^M - Y_{11}^E\right)^{-1} & -\left(Y_{21}^E\right)^{-1} \\ Y_{11}^M \cdot Y_{21}^E \cdot \left(Y_{11}^M - Y_{11}^E\right)^{-1} & -Y_{11}^E \cdot \left(Y_{21}^E\right)^{-1} \end{bmatrix}. \tag{5}$$

Inversion of (5) allows removal of the port discontinuity and L length of the connecting transmission line from the DUT. It does not allow removal of only the port discontinuity or determination of the characteristic impedance. However, it is valid for any reciprocal error box; it is not limited to pure shunt port discontinuities.

IV. Relationship of Calibration Data Sets

The three-port SOC calibration standard is nearly identical to the $2L$-length double-delay calibration standard, the only difference being that a series port is added midway between the two end ports of the double-delay $2L$-length standard. If the double-delay $2L$ through is modified by adding this third port, both a SOC and a double-delay calibration may be performed with a single modified double-delay data set.

In addition, for a shielded environment, the entire double-delay calibration data set can be derived from the SOC calibration data set, as briefly described in [5] and [6]. In detail, given the port numbering of Fig. 1(c), the Y-parameters of the $2L$ through are the (2×2) matrix forming the upper left-hand-side corner of (3), i.e., V_3 is set to zero and I_3 is discarded.

For the L-length double-delay through, we set V_2 equal to $-V_1$, placing an electric wall through the center of port 3, as in Fig. 3(b). We then remove the I_2 row as unneeded. Evaluation of I_1 and I_3 under the condition of V_3 equal to zero gives us the first column of the double-delay L-length through Y-parameters. The second column is formed from the first by symmetry yielding

$$Y_L = \begin{bmatrix} Y_{11}^S - Y_{12}^S & Y_{31}^S - Y_{32}^S \\ Y_{31}^S - Y_{32}^S & Y_{11}^S - Y_{12}^S \end{bmatrix}. \tag{6}$$

Thus, the entire double-delay calibration data set may be derived from a single SOC calibration standard.

V. Faster Evaluation of the Double-Delay Data Set

As described above, both the L- and $2L$-length double-delay calibration standards can be generated from the SOC calibration standard. Thus, when performing a double-delay calibration, one could evaluate a single SOC standard instead and derive both the L and $2L$ standards. This reduces the number of standard evaluations from two to one. However, the increase in speed is small.

If the calibration standard analysis time is limited by matrix solve and we assume that the L-length standard requires a matrix of order N and T s for analysis, then the $2L$ standard requires a matrix order of approximately $2N$ and $8T$ s for analysis. The total time required is $9T$. Eliminating the L-length standard analysis reduces this to $8T$, which is a speed increase of approximately 10%.

A substantial speed improvement is realized by analyzing two L-length standards. The first is the normal double-delay L-length through. The second is an open circuited L-length stub [see Fig. 3(c)]. The open circuit is perfect in that the stub terminates in a PMC wall. A magnetic wall is easily realized in a shielded analysis by eliminating half of the waveguide modes (those that have nonzero tangential magnetic field on the plane of symmetry) used in the shielded Green's function.

To determine the $2L$-length through Y-parameters, we also need the Y-parameters of a perfect short-circuited L-length stub. This is Y_{11} of the original L-length through. With the port 2 voltage set to zero, the end of the L-length through is connected to the perfect ground of the PEC sidewall.

With superscripts E for electric wall and M for magnetic wall, and by using methods similar to the derivation in Sec-

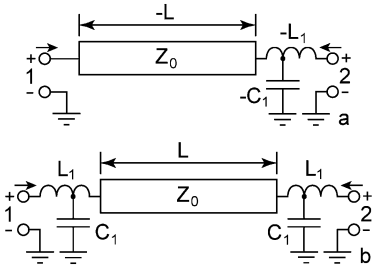

Fig. 4. Extending the SOC to calculate the naked port discontinuity without the port connecting line, invert the $ABCD$ matrix of the circuit of Fig. 3(d), yielding (a), and cascade it with an L length through, as shown in (b).

tion IV, we have the Y-parameters for the $2L$-length standard in terms of the perfect shorted and perfect open stub as

$$Y_{2L} = \frac{1}{2}\begin{bmatrix} Y_{11}^M + Y_{11}^E & Y_{11}^M - Y_{11}^E \\ Y_{11}^M - Y_{11}^E & Y_{11}^M + Y_{11}^E \end{bmatrix}. \tag{7}$$

In fact, this electric/magnetic-wall analysis approach can be used for any circuit that is symmetric about a center line, not just the $2L$-length through line described here. Alternatively and equivalently, one can directly apply the SOC to the electric- and magnetic-wall data. We use the term "equivalent" in the sense of starting with the same data and yielding the same result.

Now, both standards of the double-delay calibration are evaluated with analysis of two L-length stubs. Using the notation from above, this reduces total analysis time from $9T$ to $2T$. This represents a 350% (4.5×) faster analysis for the double-delay calibration in a shielded environment.

The SOC calibration is usually performed in an unshielded environment. If the unshielded analysis is modified to allow two types of half-space analysis, one bounded by an infinite vertical electric wall, the other bounded by an infinite vertical magnetic wall, then the SOC can enjoy a similar advantage. In fact, such data can be used directly in the SOC algorithm rather than being derived from the appropriate excitations of the three-port SOC calibration standard. An unshielded half-space analysis is easily realized by use of images.

If characteristic impedance, zero reference plane shift, or the naked port discontinuity are to be characterized, then the unshielded SOC additionally requires analysis of the L-length through in full space (in addition to a grounded half-space, as above). With this addition, the set of standards is identical to that described in the beginning of Section IV.

If images are used in an unshielded analysis to realize a half-space analysis, matrix fill time is increased. In contrast, a shielded analysis inherently includes an electric wall, and a magnetic wall is included by removing half of the Green's function, speeding the matrix fill.

VI. Extended SOC

The result of the SOC is the port discontinuity plus connecting transmission line [see Fig. 3(d)]. To extend the SOC to determine the electrical length and characteristic impedance, first invert the SOC deembedding $ABCD$ matrix yielding the circuit of Fig. 4(a).

Next, determine the circuit parameters of the double-delay L-length through [see Figs. 1(a) and 4(b)]. For shielded analysis, it can be determined directly from the SOC standard, as described in Section IV. For unshielded analysis, a second L-length standard must be analyzed. The L-length standard cannot be derived from the $2L$-length SOC standard because of the arbitrary port discontinuities.

Pre-multiply the L-length through $ABCD$ matrix by the inverted SOC deembedding $ABCD$ matrix. This yields the naked port discontinuity. The naked port discontinuity is used to deembed the L-length through, leaving just the L-length transmission line. We now have sufficient information to proceed as in Section II and deembed the DUT with either no reference plane shift, or with a shift of distance L from the port into the DUT.

An alternative way to obtain the deembedded L-length line is to invert the cascading matrix of the embedded L-length line [see Fig. 4(b)] and then post-multiply twice by the SOC port discontinuity [see Fig. 3(d)].

Now that we have the deembedded L-length line, we can determine the electrical length and characteristic impedance of the port connecting line. The significance of this is that we can now determine the characteristic impedance of a transmission line based only on port current–voltage relationships for both shielded and unshielded analysis for any arbitrary reciprocal port discontinuity.

The double-delay calibration is this extended SOC specialized to a shielded environment yielding port discontinuities with no series impedance. The original SOC is identical to this extended SOC, only lacking the L-length through and double-delay inspired matrix manipulations described here.

As for nomenclature, we refrain from introducing a new acronym for this extended SOC. Rather, we continue to refer to it as SOC. Occasionally we also refer to specializations such as shielded SOC or unshielded SOC. We strongly recommend that the term "open SOC" not be used, as it is not clear if the word "open" refers to a circuit (as it does within the acronym) or to the environment. When shielded SOC is specialized to ports that are pure shunt admittance (true for most shielded planar EM analyses in applied use today), then it is identical to double delay.

VII. Significance of TEM Equivalent Characteristic Impedance

The concept of characteristic impedance for inhomogeneous media has seen extensive discussion over the last several decades [10]–[17]. The earliest known reference to the TEM equivalent characteristic impedance is [11]. Measurements (suggestive of the SOC calibration standard) were performed in [12]. An especially detailed bibliography is provided in [17]. The basic problem is that most definitions of characteristic impedance are based on linear functionals of transverse cross-sectional fields. The functionals based on line integrals depend on the path taken for inhomogeneous media and are, thus, nonunique. The TEM equivalent characteristic impedance depends only on the current–voltage relationships observed at the infinitesimal voltage gap sources exciting the calibration through lines. These voltages and currents are unique.

When first introduced, [1] and [10], double-delay deembedding was used to determine the TEM equivalent characteristic impedance. This was not a complete solution, as the port discontinuity was specialized to a pure shunt admittance. The original SOC [2] was used to deembed a length of transmission line from which characteristic impedance was inferred [9], [14]–[16]. This solved the problem for arbitrary port discontinuities, but the determination of characteristic impedance was carried out outside of the calibration.

Now with the double-delay inspired extensions to the SOC introduced in Section VI, the SOC by itself is sufficient to uniquely determine the only characteristic impedance that is consistent with the SOC calibration standard port current–voltage relationships in the presence of arbitrary reciprocal port discontinuities. Any other value of characteristic impedance is necessarily inconsistent with the port current–voltage relationship and can thus be considered incorrect.

In [1], it was pointed out that the specialization of the port discontinuity to a pure shunt admittance precluded its exact application to measurement, as it might be difficult to realize (or at least to verify) such a port discontinuity in practice. However, now with this extended SOC, that limitation is removed.

If implemented in actual physical measurements, the SOC requires measurement of a symmetric $2L$-length through (an additional L-length through is required if characteristic impedance is desired). Since physical measurement of a series port in the center of the $2L$-length through may be difficult, we would substitute measurement of the current at the base of an L-length short-circuited stub. This type of measurement is not a standard microwave measurement, but at least there is no fundamental limitation preventing the measurement from being performed to a high level of quantifiable accuracy given sufficient resources.

We point out that this definition of characteristic impedance is preferred because it is based on port current–voltage relations, just as both microwave measurement (which is based equivalently on port transmitted-reflected wave relations) and microwave circuit analysis. Neither measurement, nor analysis has anything to do with linear functionals of transverse transmission-line fields.

VIII. Causality Validation

To verify the physical nature of the SOC derived TEM equivalent characteristic impedance, we checked the variation of characteristic impedance as a function of frequency. Specifically, if $Z_0(f)$ corresponds to a causal system, then the phase $\arg(Z_0(f))$ is directly related to the magnitude $\mathrm{mag}(Z_0(f))$ by a Hilbert transform [17]. If wide-band data is calculated, then the SOC calculated $\arg(Z_0(f))$ can be used to determine the $\mathrm{mag}(Z_0(f))$ required for a causal system. This causal $\mathrm{mag}(Z_0(f))$ is compared to the SOC calculated $\mathrm{mag}(Z_0(f))$. Differences between the two are due to error in the SOC calculation of $Z_0(f)$ and to the necessarily sampled and band-limited SOC data.

Comparing the causal $\mathrm{mag}(Z_0(f))$ to the SOC calculated result is easily effected by the use of the program CausalCat.[1]

[1]D. F. Williams, CausalCat, June 20, 2001. [Online]. Available: http://www.boulder.nist.gov/div818/81801/dylan/software.html

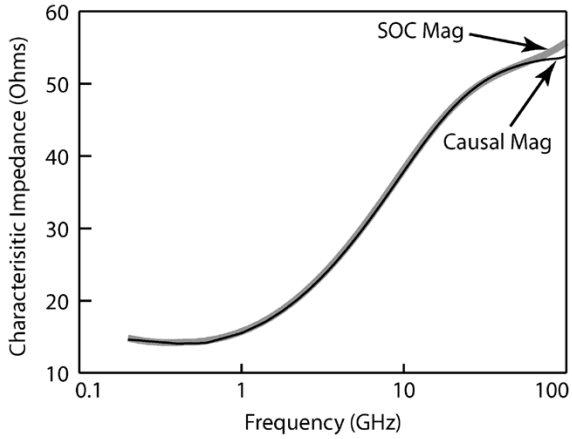

Fig. 5. Phase of the SOC calculated characteristic impedance is used to calculate the magnitude required for causality and is compared to the SOC calculated magnitude for a lossy line.

We partially verified the correctness of the program using simple test cases like lossless coax and rectangular waveguide. Significant low-frequency noise was seen for the lossless coax case, however, high-frequency lossless coax and all other cases worked well.

The most interesting case investigated is presented here. The structure is a 72-μm-wide line 1-μm-thick metal conductivity 3×10^7 S/m on top of 1-μm-thick $\varepsilon_{\mathrm{rel}}4.5$ on top of 100-μm-thick $\varepsilon_{\mathrm{rel}}11.8$ conductivity 12.5 S/m bounded on the bottom by a perfectly conducting ground plane. A one-sheet model [18] with all current assumed to be flowing on the bottom side of the actual thick line was used. Cell size is 2-μm wide and 10-μm long. The L-length through is 2000-μm long and the box is 1000 μm from one sidewall to the other across the width. There is 1000 μm of air on top just below a perfectly conducting top cover. Analysis was performed from 0.2 to 100 GHz with 41 logarithmically spaced points. The results in Fig. 5 are for ports in a shielded analysis with only shunt port capacitance, and there is no series impedance.

In spite of the very high loss and significant loss induced dispersion, the causal $\mathrm{mag}(Z_0(f))$ (calculated from the SOC $\arg(Z_0(f))$) and the SOC calculated $\mathrm{mag}(Z_0(f))$ agree almost everywhere to within several tenths of an ohm. The difference approaching 100 GHz appears to be due to the lowest box resonance at 140 GHz. When the box is made smaller, the resonance moves up and the difference at 100 GHz disappears.

When using long calibration standards, as is the case here, a problem can appear when the standard is an integer multiple of one-half wavelength long. In this case, B and C of (2) go to zero and the impedance of the line is unavailable, even though the deembedding is still valid. This is not a problem for the line described here because it is lossy and, thus, the electrical length is always complex and never equal to a pure real 180°.

The calibration standards used for Fig. 5 were modified to artificially include a series inductance. This was done by narrowing each port 1 and port 2 linewidth to 4-μm wide for a distance of 10 μm. The series inductive reactance is 20 Ω at 100 GHz. The extended SOC calibration is repeated with the results different from the pure capacitive ports on average by 0.1 Ω, peak difference is 0.4 Ω at 80 GHz.

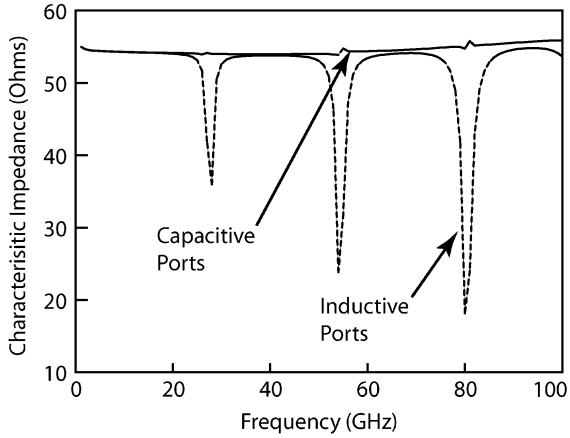

Fig. 6. When the L-length standard is a multiple of a half-wavelength long, there is difficulty deembedding both shunt capacitive (shielded) and series inductive (unshielded) port discontinuities.

The situation changes when there is low loss. We modify the geometry used for Fig. 5 by making the substrate lossless. Metal loss is retained. A full extended SOC is then used to determine characteristic impedance, as described above. Fig. 6 shows the SOC characteristic impedance result for both the pure shunt capacitive (shielded) ports and the series inductive (unshielded) ports. The sharp drops in the inductive port characteristic impedances occur when the L-length line is a multiple of a half-wavelength long. This makes sense when we realize that, at these frequencies, such a line is itself a small series inductance. The extended SOC cannot determine which of the three series inductors (two ports and one transmission line) is desired. The problem becomes worse at higher frequencies as the series port reactance increases. For this reason, if SOC is used to deembed ports with series inductance, the L-length line should be kept at approximately a quarter-wavelength long for best accuracy. If this precaution is exercised, the extended SOC may also be used to deembed local grounds [19] in an unshielded environment. Failure modes for both SOC and double delay are also detailed in [19], as well as [1], [5], and [6].

A small discontinuity is seen at the half-wave points for the capacitive port discontinuity result as well, which is due to B and C in (2) becoming small. Since both ports are pure shunt capacitances, there is less difficulty in determining the small series inductance of the half-wave-long line.

We also point out that there is no need for SOC deembedding or the local ground deembedding in [19] to be restricted to ports and connecting lines in a horizontal plane. The port connecting L-length lines may also be vertical (as in vias). This would be convenient when deembedding ports intended for connection to high-density integrated circuits, such as ball-grid arrays.

IX. Conclusion

This paper has described the unification of the double-delay and SOC deembedding algorithms useful for deembedding EM analysis results. Both algorithms are shown to be special cases of an extended SOC algorithm.

The original SOC requires only a $2L$-length standard with a third port in the center. It removes the port discontinuity and an L length of line from the DUT. In its extended version, the SOC requires an additional analysis of an L-length line. With this additional information, it can deembed just the port and determine the characteristic impedance and electrical length of the deembedding standard.

If the port discontinuity is specialized to a pure shunt admittance, as is the case with shielded analysis, then only the three-port $2L$-length SOC standard need be evaluated. The double-delay standards may be determined from this, allowing evaluation of the characteristic impedance and allowing placement of the reference plane at the port or at a distance L toward the DUT from the port.

When both electric wall and magnetic wall half-space analysis is available, the short and open L-length standards are calculated directly, resulting in a 4.5 times faster evaluation of the calibration standards. Unshielded analysis requires an additional analysis of an L-length through in open space if characteristic impedance, zero reference plane shift, or the naked port discontinuity are desired.

Applied to a shielded environment, the extended SOC provides a self-diagnostic check for deembedding failure, which is critical to assure that analysis failure is detected prior to fabrication. This check is not currently available in an unshielded environment and is highly recommended as an area of future research.

Finally, the TEM equivalent characteristic impedance, which results from the extended SOC, is shown to correspond to a causal (i.e., physical) system. The TEM equivalent characteristic impedance is the only characteristic impedance that is consistent with the current–voltage relations at the terminals of the deembedding standards.

References

[1] J. C. Rautio, "A de-embedding algorithm for electromagnetics," *Int. J. Microwave Millimeter-Wave Computer-Aided Eng.*, vol. 1, no. 3, pp. 282–287, Jul. 1991.

[2] L. Zhu and K. Wu, "Unified equivalent-circuit model of planar discontinuities suitable for field theory-based CAD and optimization of M(H)MIC's," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 9, pp. 1589–1602, Sep. 1999.

[3] M. Farina and T. Rozzi, "A short-open de-embedding technique for method of moments based electromagnetic analyses," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 4, pp. 624–628, Apr. 2001.

[4] V. I. Okhmatovski, J. Morsey, and A. C. Cangellaris, "On deembedding of port discontinuities in full-wave CAD models of multiport circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 12, pp. 2355–2365, Dec. 2003.

[5] J. C. Rautio, "Comments on 'On deembedding of port discontinuities in full-wave CAD models of multiport circuits'," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 10, pp. 2448–2449, Oct. 2004.

[6] V. I. Okhmatovski, J. D. Morsey, and A. C. Cangellaris, "Authors' reply," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 10, pp. 2449–2450, Oct. 2004.

[7] J. C. Rautio, "A time–harmonic electromagnetic analysis of shielded microstrip circuits," Ph.D. dissertation, Dept. Elect. Eng., Syracuse Univ., Syracuse, NY, 1986.

[8] J. C. Rautio and R. F. Harrington, "An electromagnetic time–harmonic analysis of shielded microstrip circuits," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-35, no. 8, pp. 726–730, Aug. 1987.

[9] L. Zhu and K. Wu, "Network equivalence of port discontinuity related to the source plane in a deterministic 3-D method of moments," *IEEE Microw. Guided Wave Lett.*, vol. 8, no. 3, pp. 130–132, Mar. 1998.

[10] J. C. Rautio, "A new definition of characteristic impedance," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1991, pp. 761–764.

[11] F. Arndt and G. U. Paul, "The reflection definition of the characteristic impedance of microstrips," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-27, no. 8, pp. 724–731, Aug. 1979.
[12] W. J. Getsinger, "Measurement and modeling of the apparent characteristic impedance of microstrip," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-31, no. 8, pp. 624–632, Aug. 1983.
[13] R. H. Jansen and N. H. Koster, "New aspects concerning the definition of microstrip characteristic impedance as a function of frequency," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1982, pp. 305–307.
[14] L. Zhu and K. Wu, "Revisiting characteristic impedance and its definition of microstrip line with a self-calibrated 3-D MoM scheme," *IEEE Microw. Guided Wave Lett.*, vol. 4, no. 2, pp. 87–89, Feb. 1998.
[15] J. Rautio, "Comments on 'Revisiting characteristic impedance and its definition of microstrip line with a self-calibration 3-D MoM scheme'," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 1, pp. 115–117, Jan. 1999.
[16] L. Zhu and K. Wu, "Authors' reply," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 1, pp. 117–119, Jan. 1999.
[17] D. F. Williams, B. K. Alpert, U. Arz, D. K. Walker, and H. Grabinski, "Causal characteristic impedance of planar transmission lines," *IEEE Trans. Adv. Packag.*, vol. 26, no. 2, pp. 165–171, May 2003.
[18] J. C. Rautio and V. Demir, "Microstrip conductor loss models for electromagnetic analysis," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 3, pp. 915–921, Mar. 2003.
[19] J. C. Rautio, "De-embedding the effect of a local ground plane in electromagnetic analysis," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 770–776, Feb. 2005.

James C. Rautio (S'77–M'78–SM'91–F'00) received the B.S.E.E. degree from Cornell University, Ithaca, NY, in 1978, the M.S. degree in systems engineering from the University of Pennsylvania, Philadelphia, in 1982, and the Ph.D. degree in electrical engineering from Syracuse University, Syracuse, NY, in 1986.

From 1978 to 1986, he was with General Electric, initially with the Valley Forge Space Division, then with the Syracuse Electronics Laboratory. During this time, he developed microwave design and measurement software and designed microwave circuits on alumina and on GaAs. From 1986 to 1988, he was a Visiting Professor with Syracuse University and Cornell University. In 1988, he joined Sonnet Software, Liverpool, NY, full time, a company he had founded in 1983. In 1995, Sonnet Software was listed on the Inc. 500 list of the fastest growing privately held U.S. companies, the first microwave software company ever to be so listed. Today, Sonnet Software is the leading vendor of three-dimensional planar high-frequency EM analysis software.

Dr. Rautio was the recipient of the 2001 IEEE Microwave Theory and Techniques Society (IEEE MTT-S) Microwave Application Award. He was appointed an IEEE MTT-S Distinguished Microwave Lecturer for 2005–2007 lecturing on the life of James Clerk Maxwell.

Vladimir I. Okhmatovski (M'99) was born in Moscow, Russia, in 1974. He received the M.S. (with distinction) and Candidate of Science (Ph.D.) degrees from the Moscow Power Engineering Institute, Russia, in 1996 and 1997, respectively.

In 1997, he joined the Radio Engineering Department, Moscow Power Engineering Institute, as an Assistant Professor. From 1998 to 1999, he was a Post-Doctoral Research Associate with the National Technical University of Athens. From 1999 to 2003, he was a Post-Doctoral Research Associate with the University of Illinois at Urbana-Champaign. From 2003 to 2004, he was with the Department of Custom Integrated Circuits Advanced Research and Development, Cadence Design Systems Inc. He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, University of Manitoba, Winnipeg, MB, Canada. He has authored and coauthored over 30 papers in professional journals and conference proceedings. His research interests are the fast algorithms of computational electromagnetics and modeling of high-speed digital circuits and mixed-signal components.

Dr. Okhmatovski was the recipient of the Governmental and Presidential Scholarships of the Russian Federation in 1995 and 1996, respectively, and a 1997-2000 Scholarship of the Russian Academy of Science. In 1996, he was the recipient of the Best Young Scientist Report Award presented at the VI International Conference on Mathematical Methods in Electromagnetic Theory (MMET'96). He was also the recipient of the Outstanding Technical Paper Award at the Third Electronics Packaging Technology Conference (EPTC 2000).