

# Digital Signals Integrity Tutorial

## Sonnet Microstrip Models



The College of New Jersey

**Thanks to Sonnet's Application Engineer, Greg Kinnetz and the TCNJ Spring 2014 ELC 441 Digital Engineering Systems Class,**

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# Digital Engineering Systems

## Outline

- Digital Design Introduction & Design Rules
- What are the Issues of HS Digital Design Today?
- Relationship between Time and Frequency Domain
  - Rise Time and Fourier Frequency Components
  - Digital Square Wave Generates Odd Harmonics
  - Relationship between the Logic Rise Time and Frequencies Generated
- Electromagnetic Modeling of PCB Traces
- PCB Microstrip Example
- EM Modeling of Transmission Lines (PCB Traces on FR4) using Sonnet
  - SONNET Tutorial 1 – Terminated Microstrip Line => Build on FR4, Graph S11 in dB, Plot VSWR, Impedance on a Smith Chart,
  - SONNET Tutorial 2 – Coupled Microstrip Lines => Plot the Near End Crosstalk (NEXT) using the dB[S21] S-parameter, Current Density
  - SONNET Tutorial – Differential Pair Microstrip Lines => Extract S, Y, Z-parameter, Pi-model, N-coupled, Broadband, and Inductor Files
- Conclusions of Sonnet as a Digital Signals Integrity Simulation Tool
- SI Verification Tool – Time Domain Reflectometry
- SI Verification Tool – Eye Diagram Mask
- SI Verification Tool – Bit Error Rate Tester (BERT)
- SI Verification Tool – Vector Network Analyzer (VNA)
- Tutorial Conclusions
- Text References:
  - Hall, Hall, and McCall, *High-Speed Digital System Design*, John Wiley & Sons Inc., 2000
  - Johnson and Graham, *High Speed Signal Propagation*, Prentice Hall, 2003

# Advanced Digital Design Introduction

## Digital Design Introduction & Design Rules

**The design guidelines today for high-speed Digital Signal Integrity require, as standard:**

- All PCB traces need to be terminated at a controlled impedance
- Reduce Impedance & inductive elements in the return path
- Avoid Branched Routing Topology
- Design Low-Impedance ground and power distribution paths
- Understand how Connectors and Vias change the impedance

**Note:** Beginning digital engineers often make a mistake in not terminating the input – ALL High-impedance (Hi-Z) inputs must be terminated otherwise intermittent results can occur and/or Electro-static Discharge (ESD) can damage the IC.

# Advanced Digital Design Introduction

## What are the Issues of HS Digital Design Today?

### Digital Problems are Manifest in Many Ways and Potential Root Cause Indicated:

- Specific “ONE” bits are read as “ZERO” or
- Transmitted “ZERO” bits are read as “ONE”

Intersymbol Interference (ISI) due to Impedance Mismatch

Impedance Discontinuities

Ground Loop,  $di/dt$

- Jitter (Timing Jitter)

Thermal Noise

Cross Talk

Noisy Ground Connections

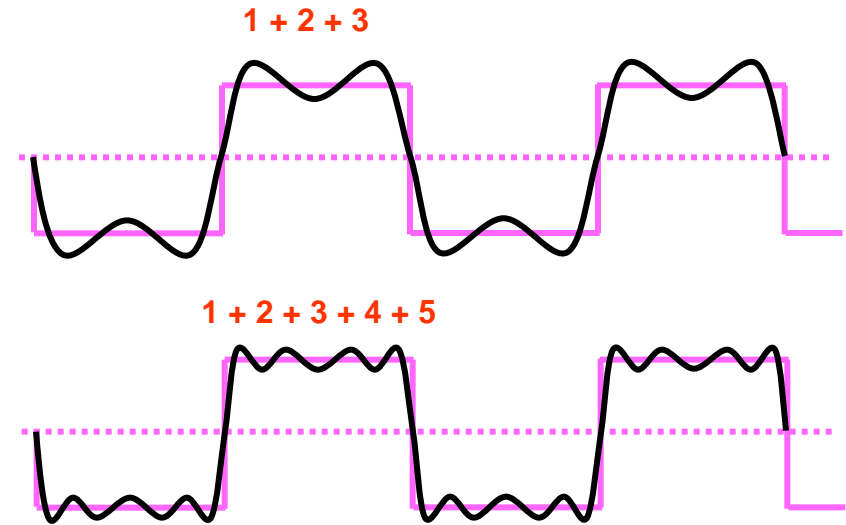
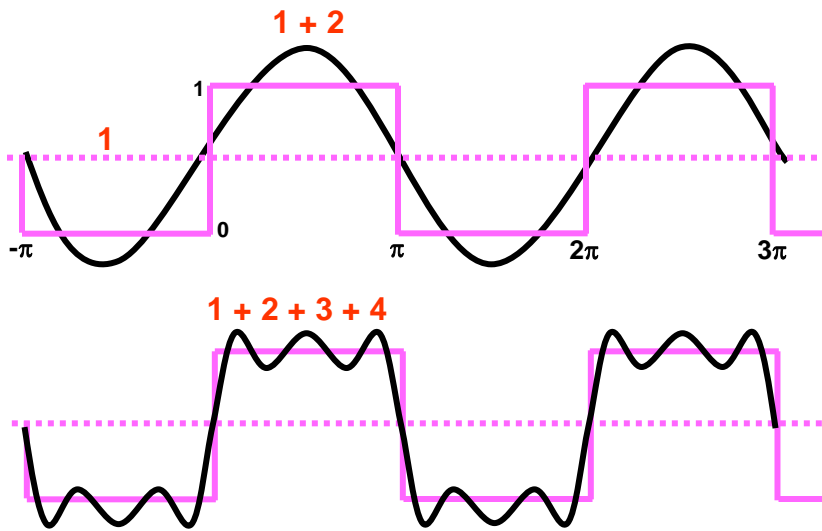
**Jitter testing** is of growing importance to engineers, as system clock frequencies are increasing inducing intersymbol interference. Current motherboards have high-speed serial bus architectures with rise time of  $<170$  picoseconds and also engineering attention has to be focused on proper buss termination.

# Relationship between Time and Frequency Domain

## Fourier Frequency Components

**FOURIER SERIES** – Digital Signals are composed of an infinite number of sinusoidal functions

**A SQUARE WAVE:**  $Y = 0$  for  $-\pi < x < 0$  and  $Y=1$  for  $0 < x < \pi$ .



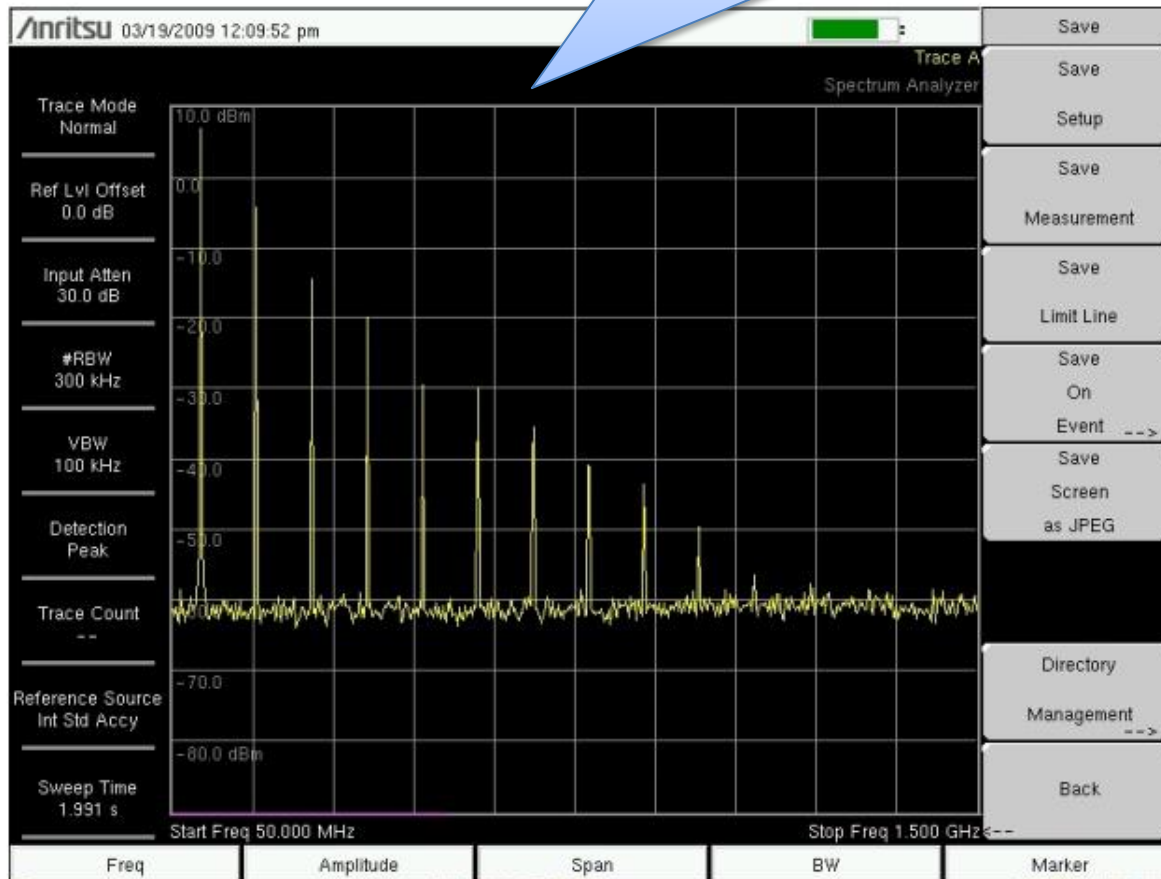
$$f(t) = \frac{2}{\pi} \sum_{n=1,3,5\dots} \frac{1}{n} \sin 2\pi n F t$$

<sup>1</sup> Hall, Hall, and McCall, *High-Speed Digital System Design*, John Wiley & Sons Inc., 2000: 284 - 303

# Relationship between Time and Frequency Domain

## Digital Square Wave Generates Odd Harmonics

Actual Spectrum plot generated by Digital Square Waves which illustrates the Frequencies Generated by a 100ps rise time (Tr of ECL Logic Family)

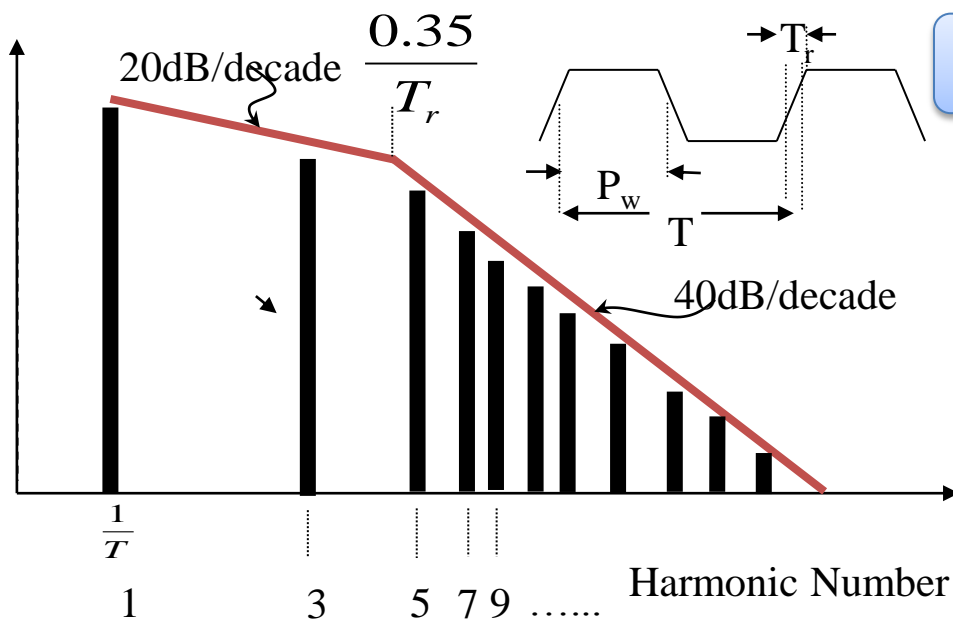


$$f(t) = \frac{2}{\pi} \sum_{n=1,3,5\dots} \frac{1}{n} \sin 2\pi n F t$$

<sup>1</sup> Hall, Hall, and McCall, *High-Speed Digital System Design*, John Wiley & Sons Inc., 2000: 85

[Weisstein, Eric W. "Fourier Series--Square Wave." From MathWorld--A Wolfram Web Resource.](http://mathworld.wolfram.com/FourierSeriesSquareWave.html)

# Relationship between the Logic Rise Time and Frequencies Generated



## Estimating the Frequency Content in a Digital Square Wave

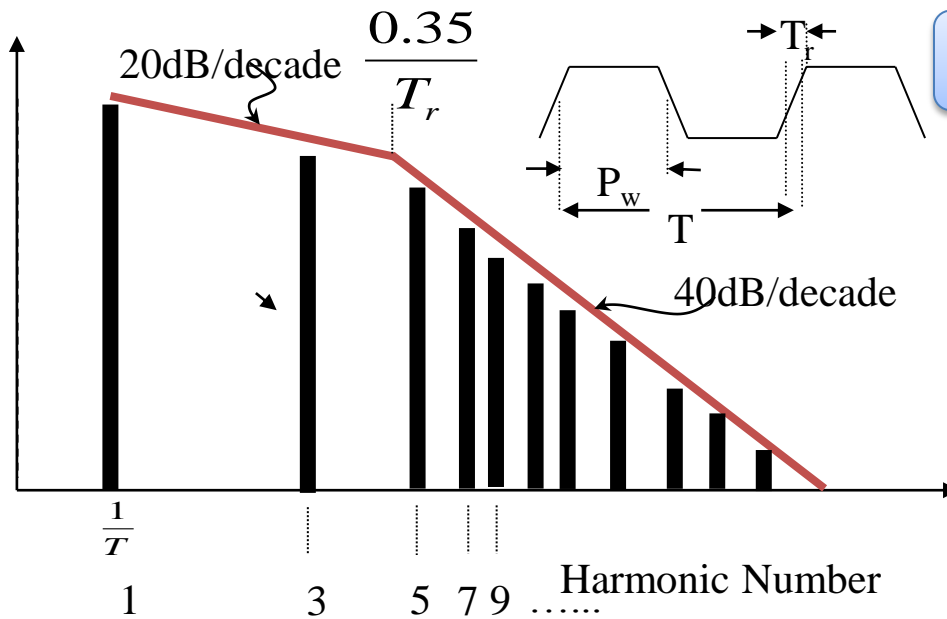
### What Frequencies and Amplitudes are Generated?

The 10%-90% rise time,  $T_r$ , is the key specification for determining the Fourier frequency components and the amplitude. For example,  $T_r$  of ECL is approximately 100nsec which, using the rule of thumb,  $350\text{MHz}/T_r = 3.5\text{ GHz}$

## The Rise Time of Modern Logic Generates MICROWAVE Frequency Components

| DIGITAL LOGIC FAMILY                                    | TYPICAL RISE TIME | CALCULATED SIGNAL BW |
|---|-------------------|----------------------|
| Transistor Transistor-Logic (TTL)                       | 15 ns             | 24 MHz               |
| Low-Power Schottky TTL (LSTTL)                          | 2 ns              | 175 MHz              |
| Complementary Symmetry Metal Oxide Semiconductor (CMOS) | 1.5 ns            | 230 MHz              |
| Gunning Transceiver Logic (GTL)                         | 1 ns              | 350 MHz              |
| Low-Voltage Differential Signaling (LVDS)               | 400 ps            | 875 MHz              |
| Emitter-Coupled Logic (ECL)                             | 100 ps            | 3.50 GHz             |
| Gallium Arsenide Logic (GaAs)                           | 40 ps             | 8.75 GHz             |

# Relationship between the Logic Rise Time and Frequencies Generated



## Estimating the Frequency Content in a Digital Square Wave

$$t_{10-90\%} = \frac{0.35}{F_{3dB}}$$

The frequency response of the digital network determines the resulting rise or transition time. The majority of the spectral energy content, as shown on the left, will be contained below  $F_{3dB}$

How do we get this Rule-of-Thumb Rise Time to Frequency Equation?  $F = \frac{0.35}{T_r}$

It can be derived from the response of a step function into a filter & time constant tau:

$$V = V_{input}(1 - e^{-t/\tau})$$

Setting  $V=0.1V_{input}$  and  $V=0.9V_{input}$ , calculate the 10-90% risetime in terms of the time constant

$$t_{10-90\%} = t_{90\%} - t_{10\%} = 2.3\tau - 0.105\tau = 2.195\tau$$

The frequency response of a 1 pole network is  $F_{3dB} = \frac{1}{2\pi\tau} \rightarrow \tau = \frac{1}{2\pi F_{3dB}}$

Substituting into the step response yields:  $t_{10-90\%} = \frac{1.09}{\pi F_{3dB}} = \frac{0.35}{F_{3dB}}$

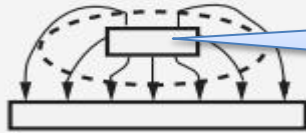


# Electromagnetic Modeling of PCB Traces

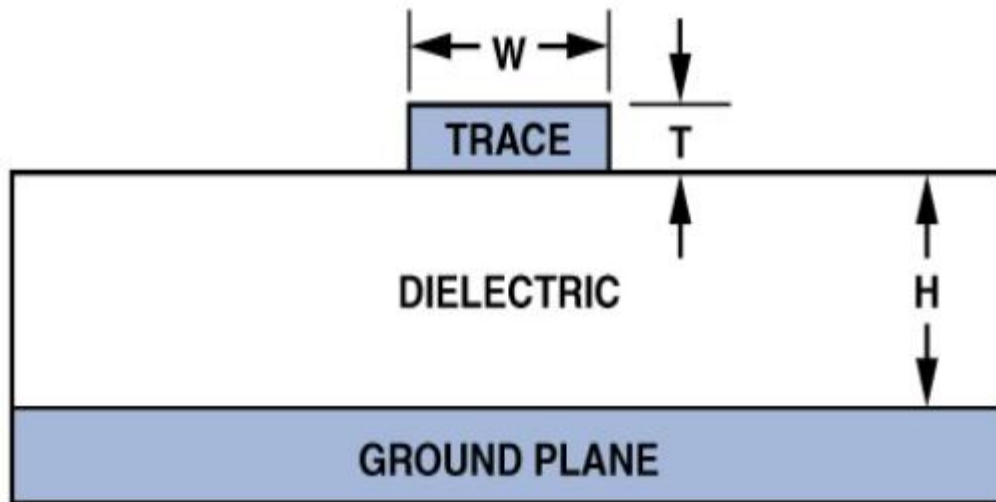
- Microstrip is a commonly used transmission line configuration in a mixed signal Printed Circuit Board (PCB) designs.
- There are closed form equations that are useful for initial transmission line calculations
- Most practical PCB circuits are quite complex and quickly exceed the limitations of the equations.
- For a more complete understanding of transmission line based circuits, an electromagnetic (EM) model is required.
- Sonnet is a useful tool for Planar EM Simulation.

# Advanced Digital Design Introduction

## PCB Microstrip Example



Sketch of the Electric and Magnetic Fields surrounding the trace "wire" on an FR4 substrate



Microstrip transmission lines are often found on the top and bottom layers of PCB's. They consist of a trace with a dielectric material and groundplane below. The trace might be exposed to air above it or covered with soldermask.

There are numerous equations in papers, books, and software calculators, which yield good initial values for microstrip transmission line quantities. One of the most important is the Characteristic Impedance  $Z_0$ . A decent rule of thumb is that the width of a microstrip trace should be approximately twice the dielectric layer height in order to produce a  $Z_0$  of 50 Ohms. This assumes an FR-4 dielectric material, which has an approximate Relative Permittivity of 4.4.

<sup>1</sup> Hall, Hall, and McCall, *High-Speed Digital System Design*, John Wiley & Sons Inc., 2000: 7 - 41

# Advanced Digital Design Introduction

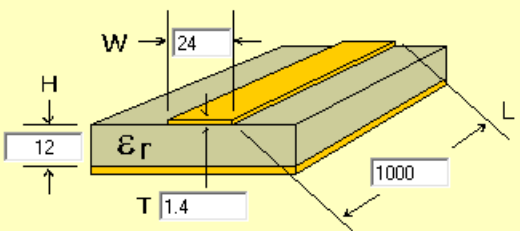
## PCB Microstrip Example

AppCAD - [Microstrip]

File Calculate Select Parameters Options Help

Microstrip

Calculate Z0 [F4]



W 24

H 12

$\epsilon_r$

T 1.4

L 1000

Dielectric:  $\epsilon_r =$  4.4

-> Enter custom Er value

Frequency: 1 GHz

Length Units: mils

Z0 = 47.11  $\Omega$

Elect Length = 0.153  $\lambda$

Elect Length = 55.0 degrees

1.0 Wavelength = 6539.958 mil

Vp = 0.554 fraction of c

$\epsilon_{eff} =$  3.257

W/H = 2.000

Normal

Click for Web: APPLICATION NOTES - MODELS - DESIGN TIPS - DATA SHEETS - S-PARAMETERS

Here is a screenshot from the freely available AppCAD program from Agilent/Avago<sup>1</sup>. In it dimensions for a microstrip transmission line have been entered and the Z<sub>0</sub> computed. Note that the rule of thumb ( $W=2*H$ , for 50 Ohms Z<sub>0</sub>) is fairly accurate.

National Instruments/AWR offers a similar program called TXLINE.

<sup>1</sup> AppCAD Utility Page: <http://www.avagotech.com/pages/appcad>

# Electromagnetic Modeling of Transmission Lines using Sonnet

- Sonnet uses a Method of Moments analysis technique to generate frequency domain data for transmission line structures.
- The particular EM solver formulation is laterally closed, which places Perfect Electric Conductor (PEC) shielding walls around the modelspace.
- It is straightforward to create or import circuit layouts in Sonnet.
- There is even a no-cost version of Sonnet (Sonnet Lite), which we will use in the following slides, to analyze some basic PCB transmission line structures. (Sonnet Lite 14.53 is used).
- For more information and to download Sonnet Lite, please visit the Sonnet Lite website at:  
<http://www.sonnetsoftware.com/products/lite/>.
- Please see the Sonnet documentation for detailed help to get started and setup models.

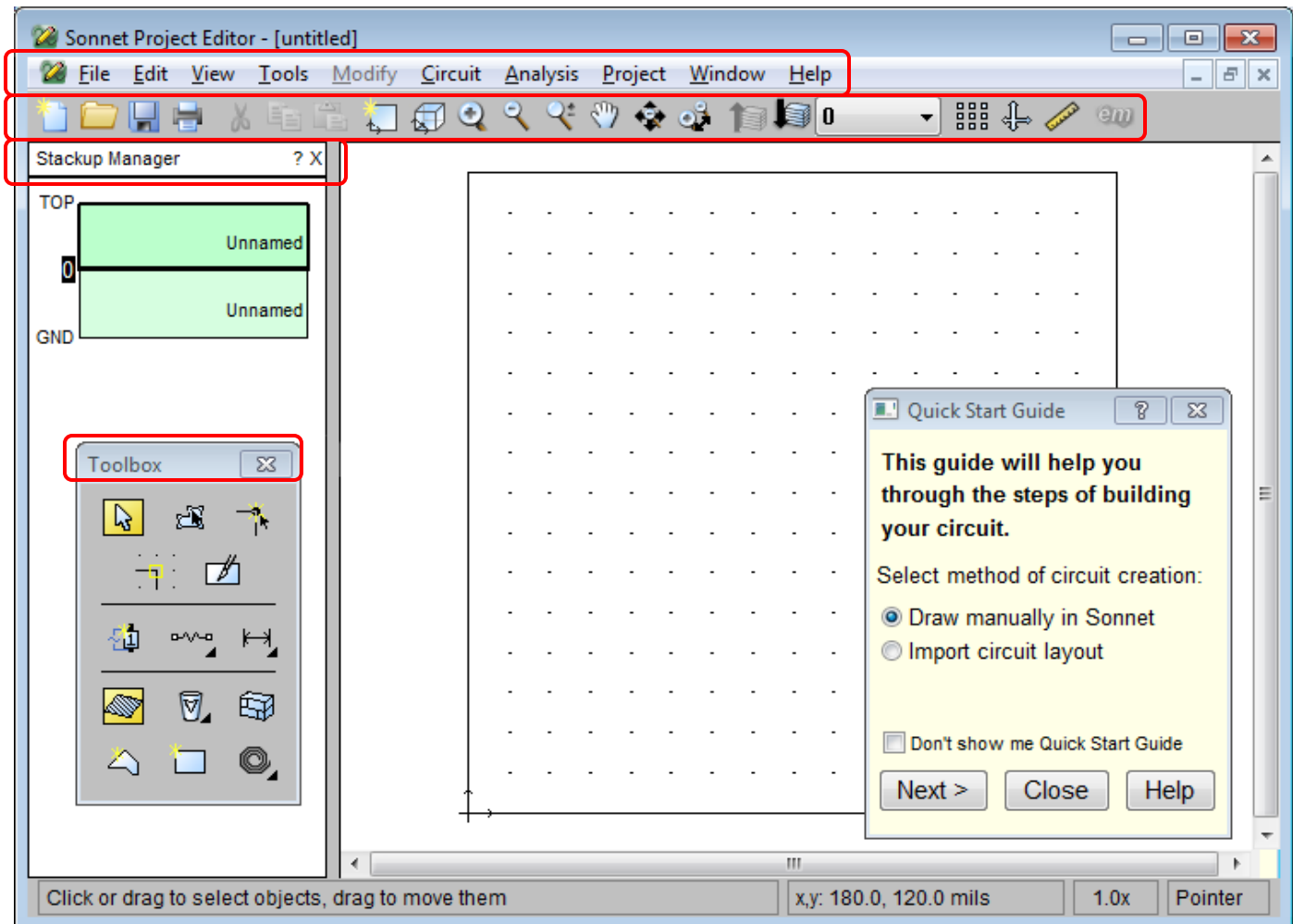
# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

This exercise will go through the creation of a simple microstrip transmission line terminated in a ideal, 50 Ohms resistor. We will use the dimensions and materials noted on the previous slides.

The purpose is to acquaint beginners with the basic use of Sonnet to design and analyze transmission lines for various purposes.

When you open a new project a blank layout window will appear. There is a Quick Start Guide window that can assist in model creation. To keep the interface clear we won't use the Quick Start Guide in this tutorial and instead use the highlighted Menu Bar, Tool Bar, Tool Box, and Stackup Manager



# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

The first step is to use the menu command **Circuit => Units** and ensure the desired units are set. We will use a length unit of mils so the default setting is correct.

At this point it is a good idea to save the project under a meaningful name. Please continue to save the project at various points after making changes.

Units-untitled

Unit Definitions

|             |      |                  |         |
|-------------|------|------------------|---------|
| Length      | mils | Frequency        | GHz     |
| Resistance  | Ohms | Conductivity     | S/m     |
| Inductance  | nH   | Resistivity      | Ohm-cm  |
| Capacitance | pF   | Sheet Resistance | Ohms/sq |

☐ Remember settings

Applying new units will:

- ☒ Maintain Physical (example: 10mm length converts to 1 cm)
- ☐ Maintain Value (example: 10 mm length converts to 10 cm)

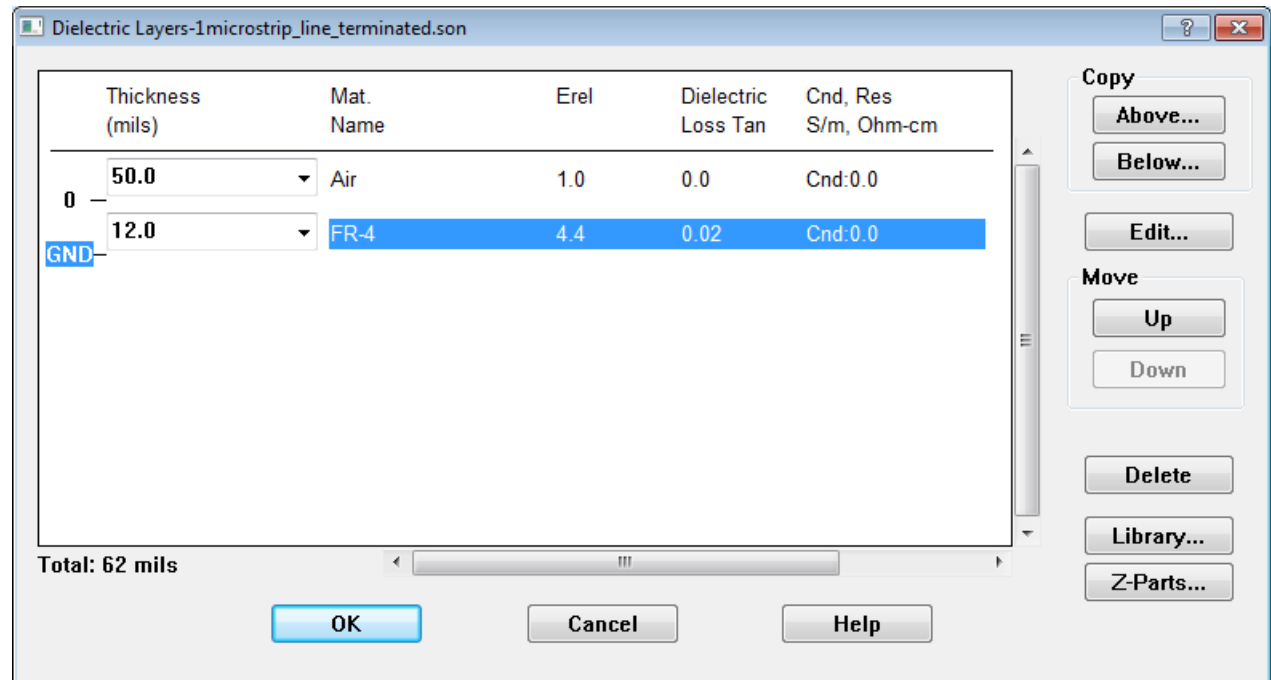
OK Cancel Help

# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

The next few steps do not necessarily have to be completed in a specific order. We will define the dielectric layers next. This dialog box can be accessed using the menu command Circuit -> Dielectric Layers or right click on the Stackup Manager and select the same command.

In this example, we need to manually enter an Air layer and FR-4 material from the library. Layer thicknesses are not stored in the library and must be manually entered.

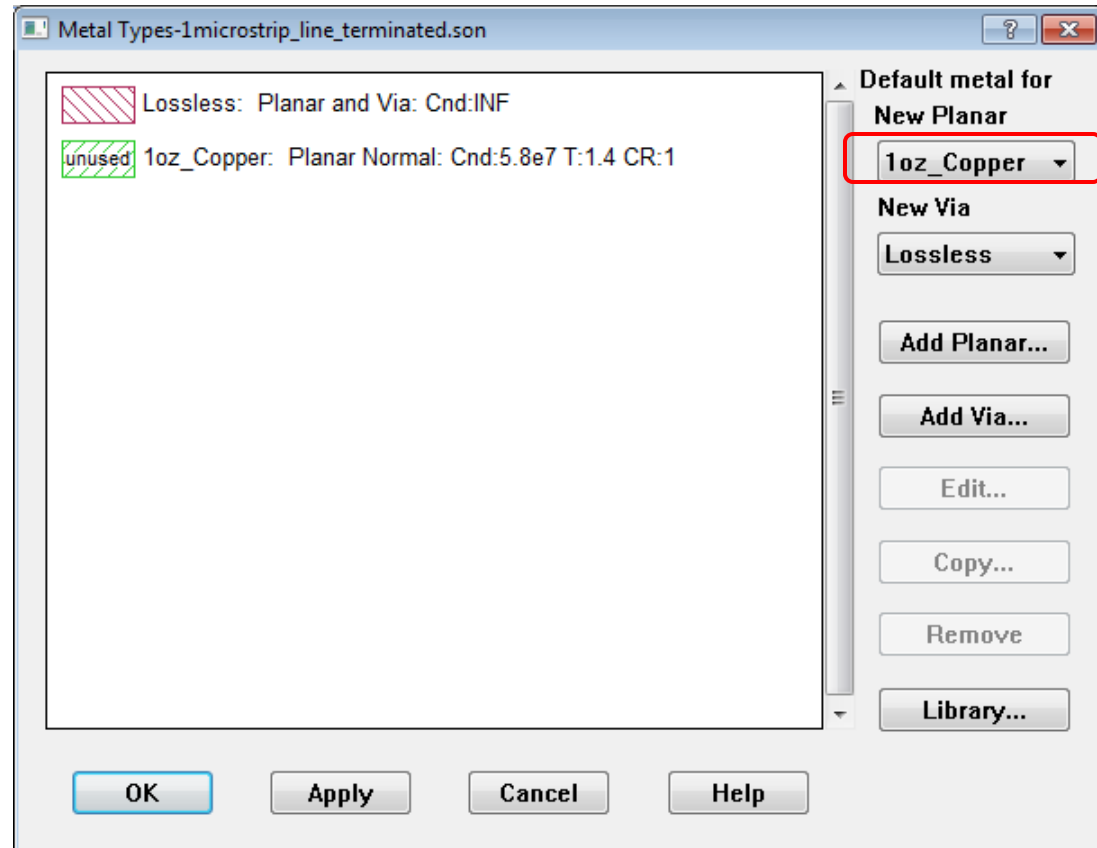


# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

We will define the metal type next. This dialog box can be accessed using the menu command Circuit -> Metal Types or right click on the Stackup Manager and select the same command.

In this example, we need to define a 1oz Copper metal type using the Add Planar button. Once this is defined, we can save some time in the future by assigning the "1oz\_Copper" metal type for new planar metal in the pulldown list.





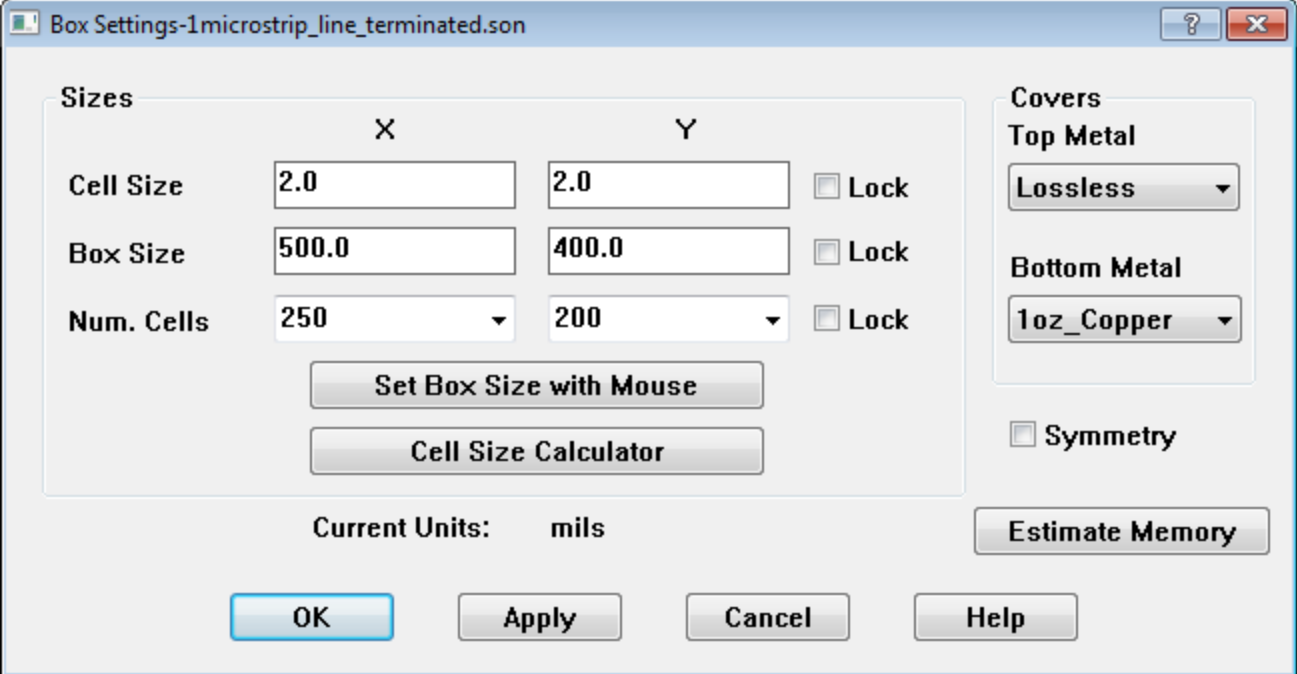
# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

We will define the analysis box next. This sets the X x Y size of the dielectric layers. This dialog box can be accessed using the menu command Circuit -> Box

In this example, we will use a 500 x 400 mil box size and a 2 x 2 mil cell size (grid). The idea is to have a large enough PCB size to allow for your circuit and use a fine enough grid to handle the dimensions you plan to use. The grid size is inversely proportional to the model size, so it must be selected carefully.

We can also set the top and bottom cover metal types. In this example, we will set the bottom cover to the 1oz\_Copper metal type to capture lossy groundplane effects in the model.



The image shows a screenshot of the 'Box Settings' dialog box in Sonnet software. The title bar reads 'Box Settings-1microstrip\_line\_terminated.son'. The dialog is divided into several sections:

- Sizes:** A table with columns for 'X' and 'Y' dimensions. It includes input fields for 'Cell Size' (2.0), 'Box Size' (500.0), and 'Num. Cells' (250 for X, 200 for Y). Each row has a 'Lock' checkbox.
- Covers:** A section on the right with dropdown menus for 'Top Metal' (set to 'Lossless') and 'Bottom Metal' (set to '1oz\_Copper').
- Buttons:** 'Set Box Size with Mouse' and 'Cell Size Calculator' are located below the size inputs. 'OK', 'Apply', 'Cancel', and 'Help' are at the bottom.
- Other:** A 'Symmetry' checkbox is present, and an 'Estimate Memory' button is at the bottom right.

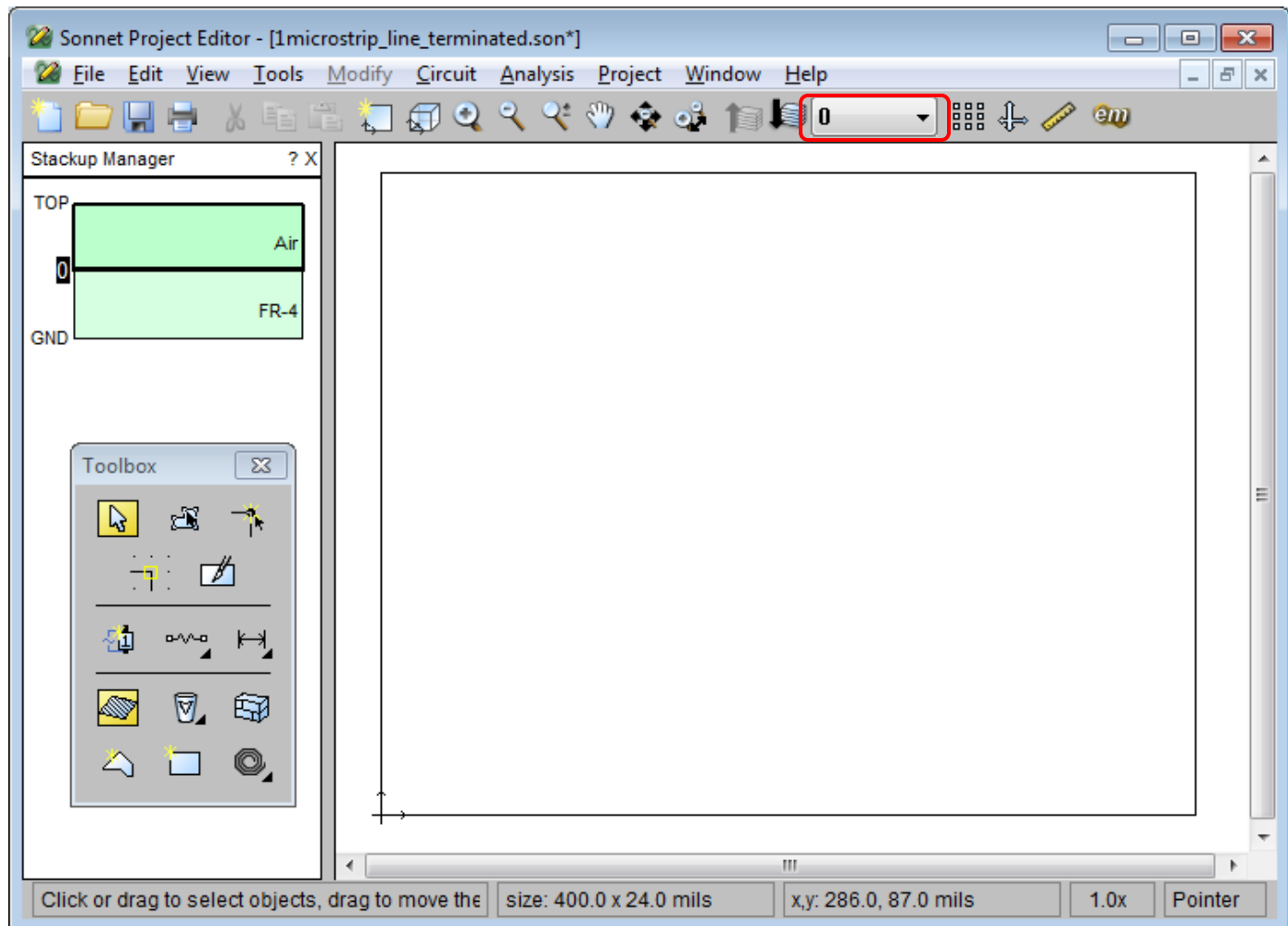
|            | X     | Y     |                               |
|------------|-------|-------|-------------------------------|
| Cell Size  | 2.0   | 2.0   | <input type="checkbox"/> Lock |
| Box Size   | 500.0 | 400.0 | <input type="checkbox"/> Lock |
| Num. Cells | 250   | 200   | <input type="checkbox"/> Lock |

Current Units:    mils

# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

The project should look like the image shown here. Ensure the Level indicator is set to "0" and then we can begin adding the traces.



# Advanced Digital Design using Sonnet

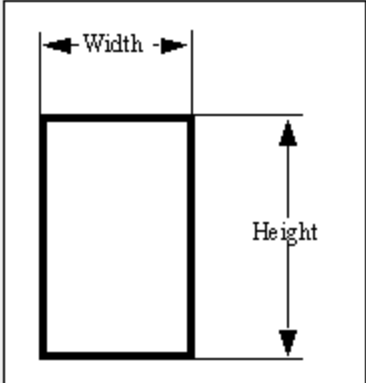
## SONNET Tutorial – Terminated Microstrip Line

We are ready to draw the traces now. There are numerous commands than can be used to create layouts inside Sonnet. You can also import existing layouts using the available translators.

We will use the command Tools -> Add Metallization -> Rectangle. Enter the values 400 and 24 as shown in the image.

Rectangle Attributes

|        |                                    |
|--------|------------------------------------|
| Width  | <input type="text" value="400.0"/> |
| Height | <input type="text" value="24.0"/>  |



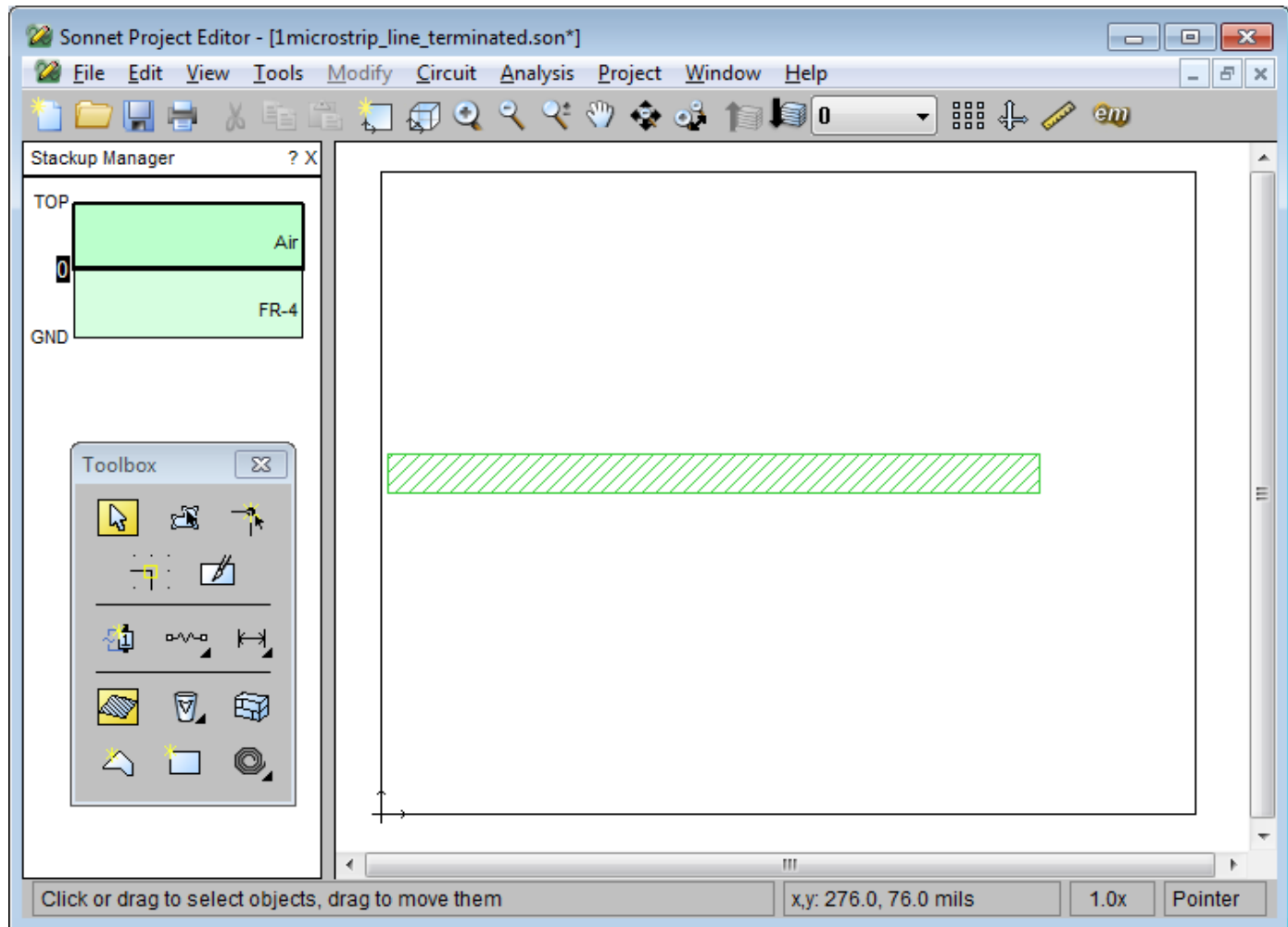
OK Cancel Help

The diagram shows a rectangle with a horizontal double-headed arrow above it labeled 'Width' and a vertical double-headed arrow to its right labeled 'Height'.

# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

The project should look something like the image shown here.

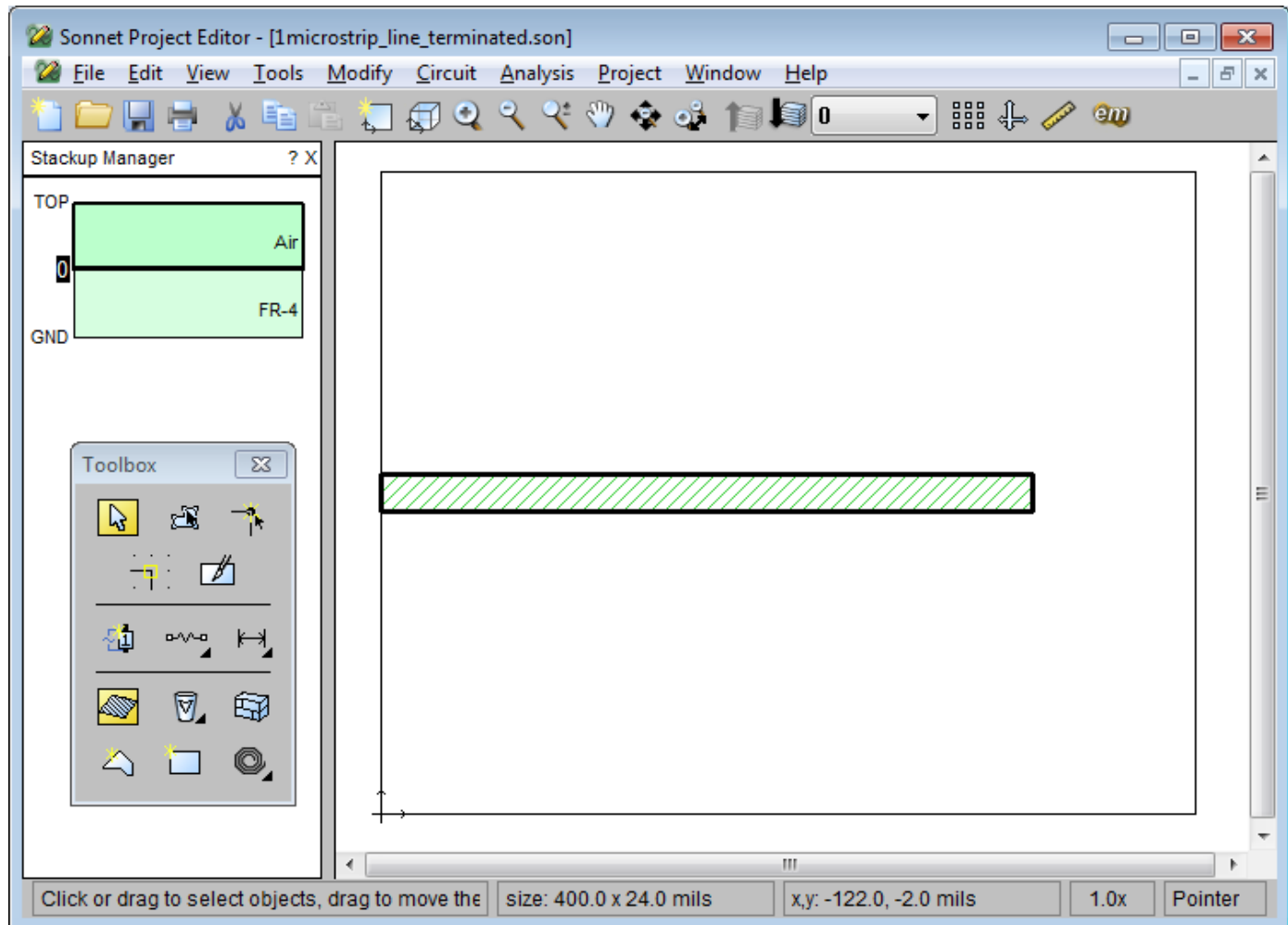


# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

To position the trace more precisely, we can select it and then use the menu command **Modify -> Center -> Vertically**. We can also use the keyboard and enter “@” and then the x,y coordinate for a relative move. Yet another way to move the polygon one grid at a time is to use the keyboard command **Shift arrow up**, **Shift arrow left**, etc.

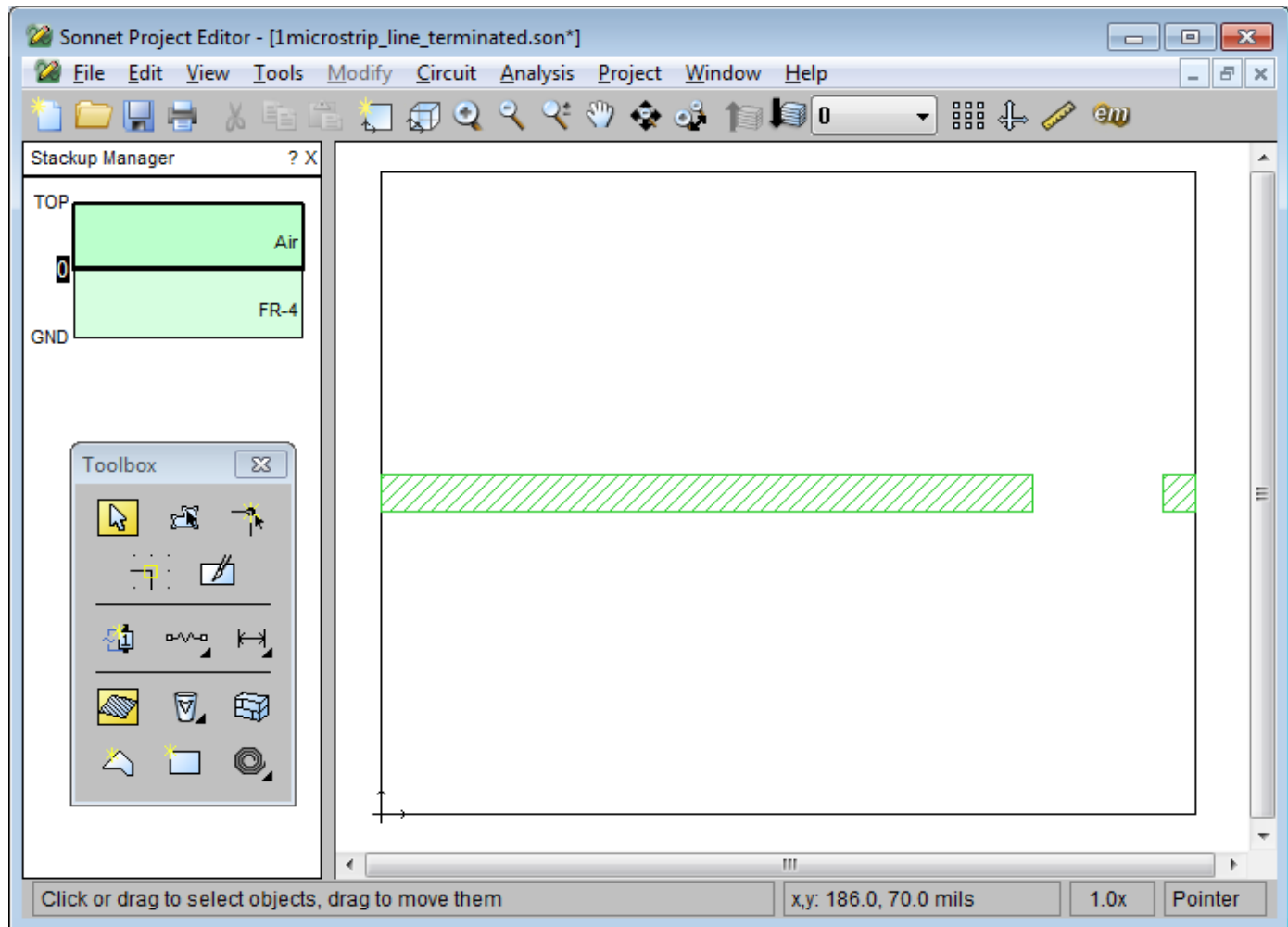
The goal is to have the trace centered and have the left edge against the substrate edge.



# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

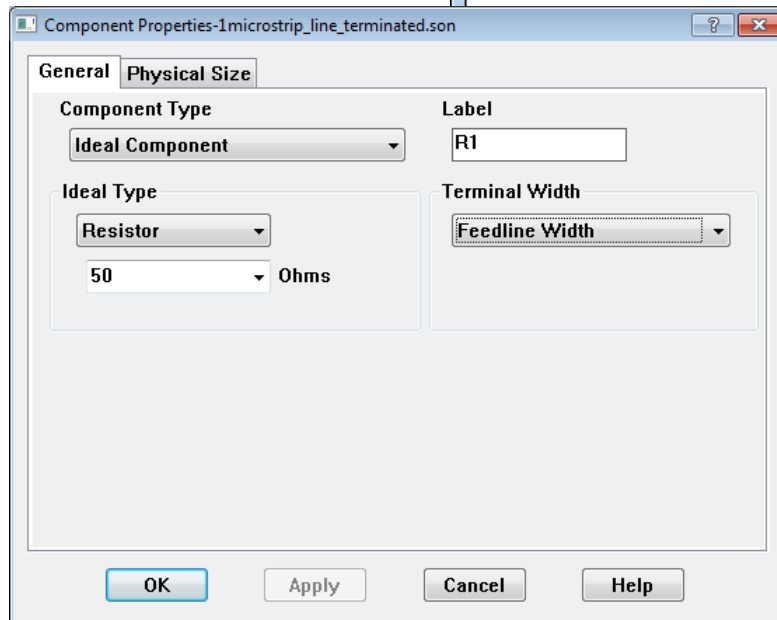
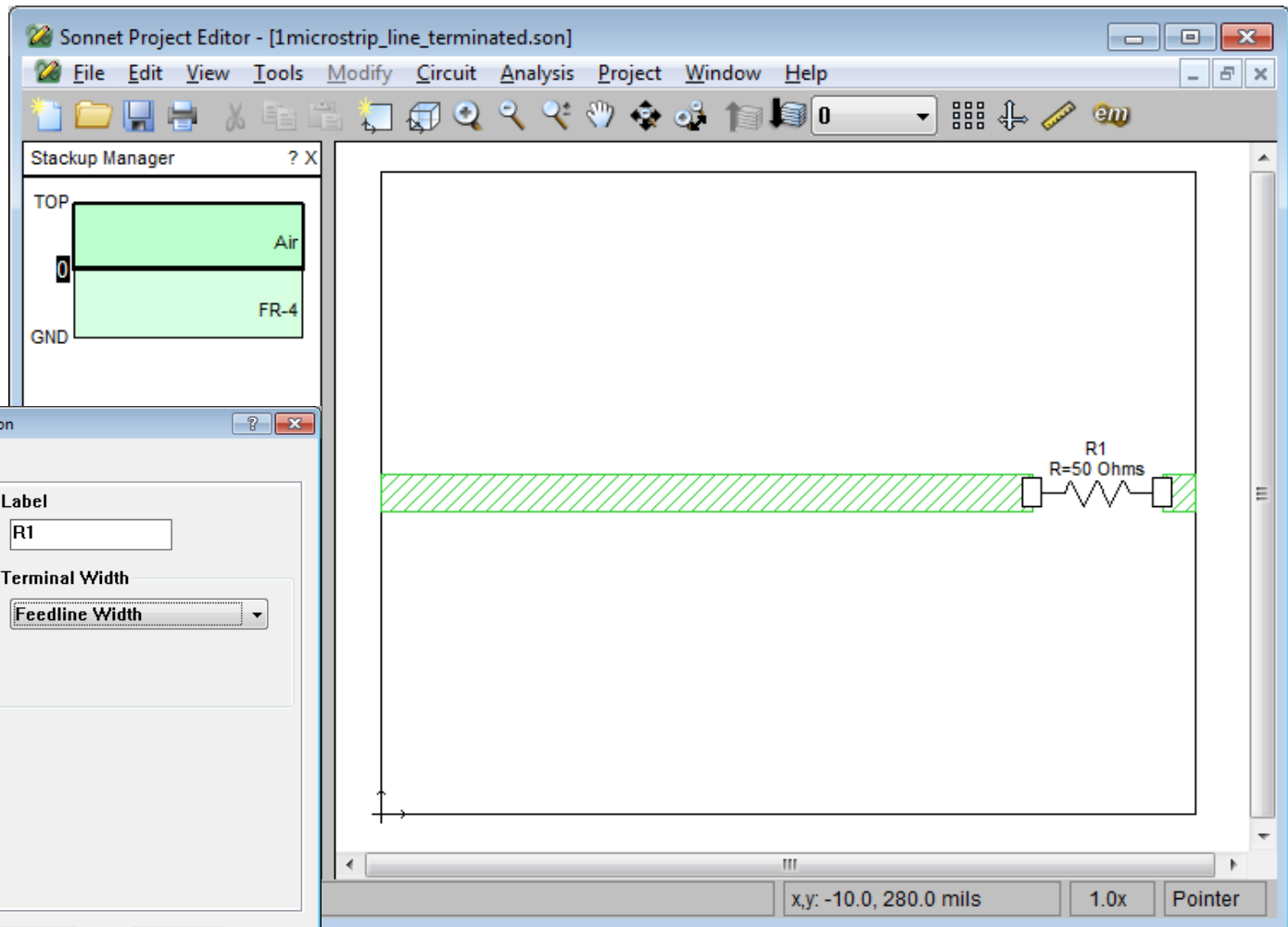
Use similar steps to add a 20 x 24 mil polygon and position it against the right edge of the substrate



# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

Use the menu command Tools -> Add Component -> Ideal, and add a 50 Ohms resistor across the gap. This resistor will function as a termination for the microstrip line.



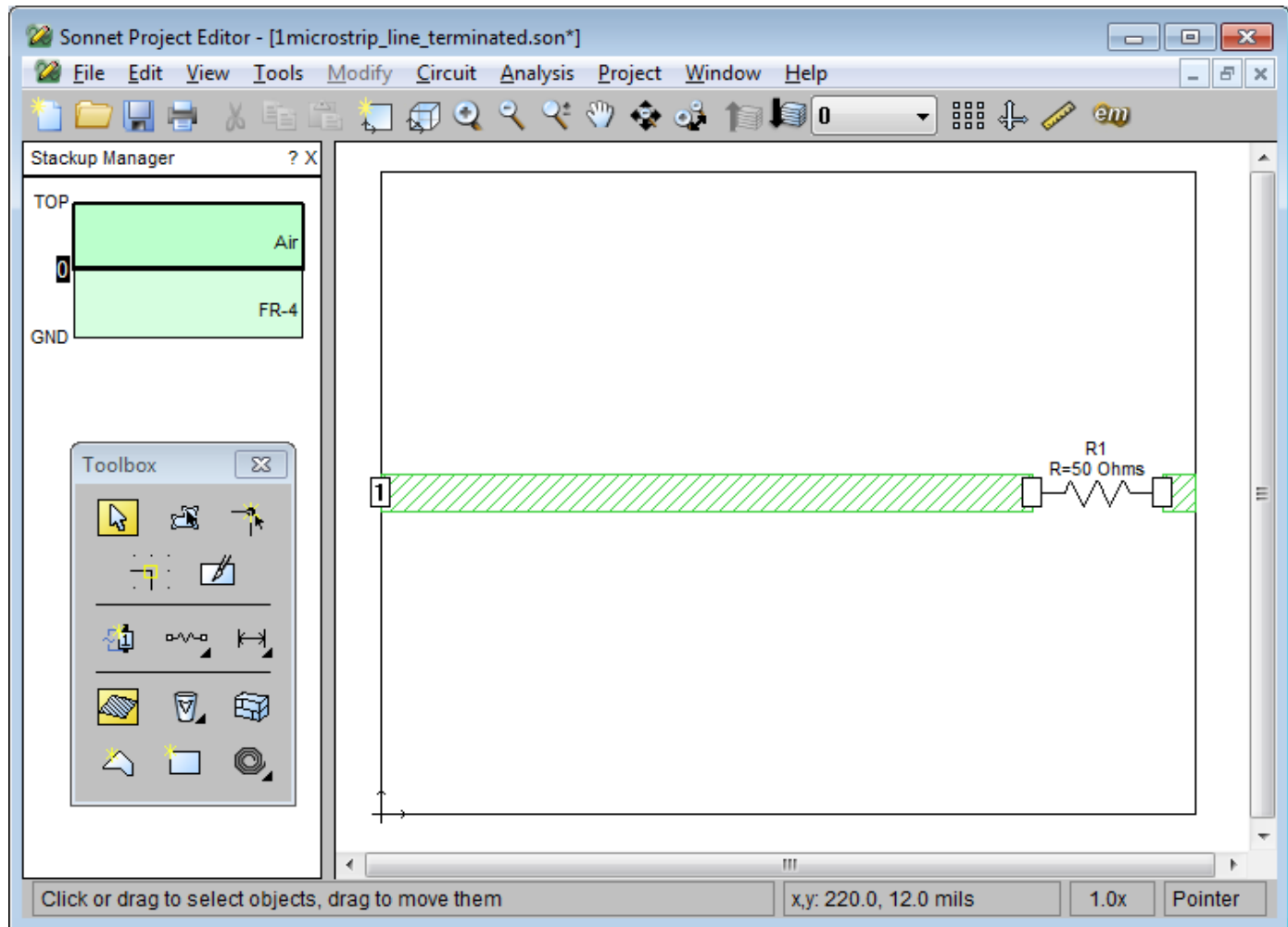
# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

Use the menu command Tools -> Add Port add a port to the left edge of the trace. This port will behave as a Boxwall Port.

The port is inserted in an infinitesimally small gap between the edge of the trace and the analysis boxwall. The positive terminal of the port source connects to the trace edge and the negative terminal to the boxwall.

This port configuration causes the analysis boxwalls and potentially the box covers to be in the return current path and behave as a ground.



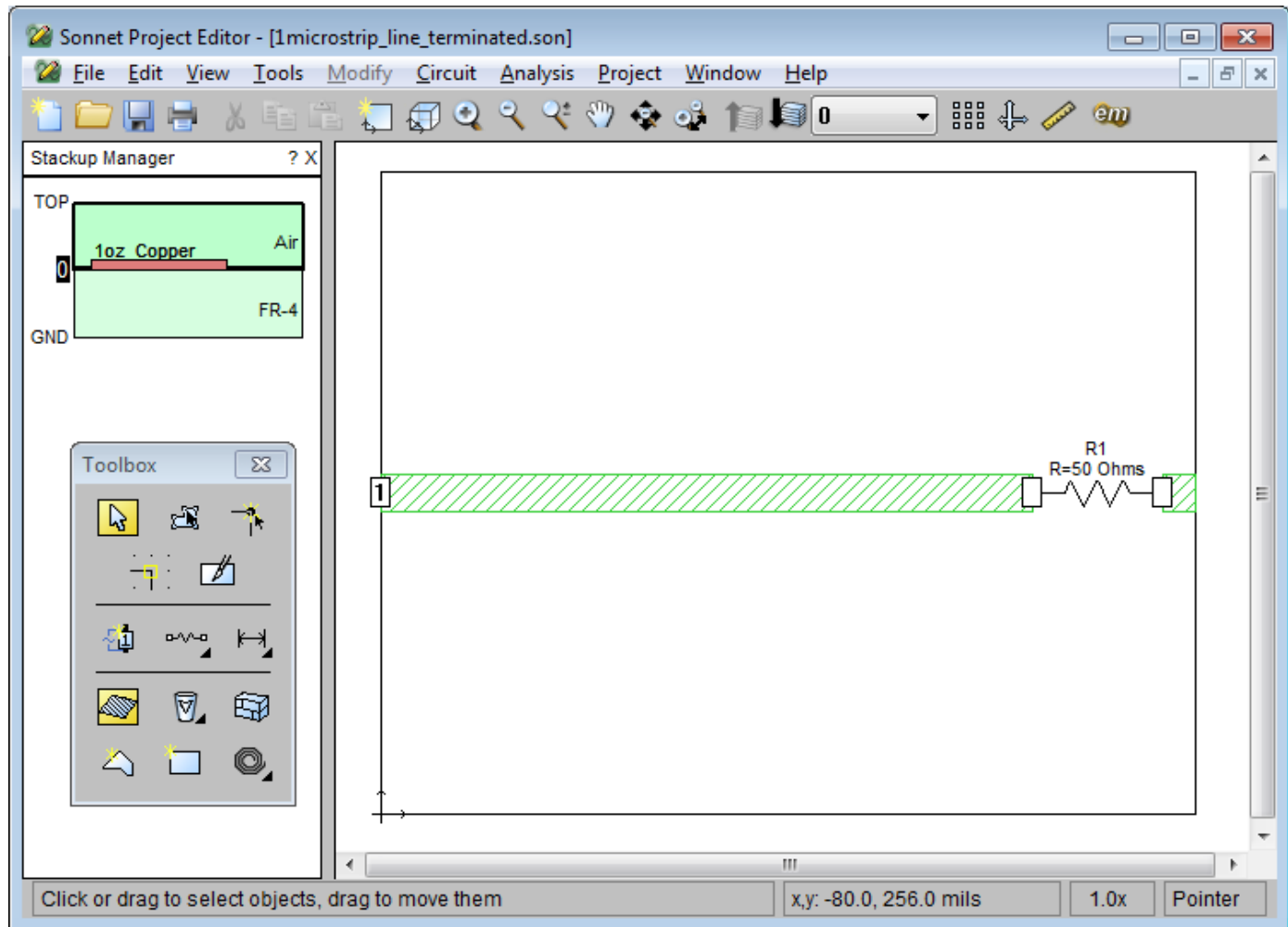


# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

To make the Stackup Manager view more complete, we can right click on it and select Auto Create Tech Layers. This will place a Tech Layer in the stackup for the metal we created.

Technology Layers are similar to drawing layers that are found in various circuit layout and CAD tools. They provide a means to assign attributes to all polygons on a layer.

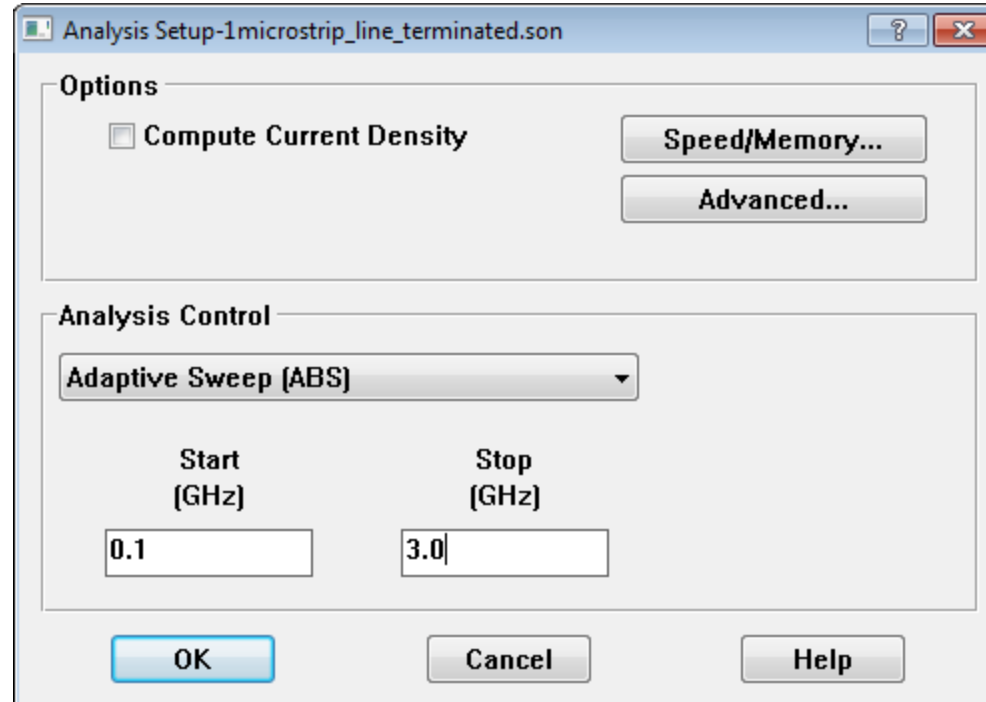


# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

To complete the model setup, we need to specify a frequency sweep. We will use the default ABS sweep over a range of 0.1 to 3.0 GHz.

The ABS sweep uses an interpolation technique, where a limited number of frequency points are fully analyzed and fitted to equations. Once enough points have been analyzed, the full wideband response is computed, with a fine frequency step.



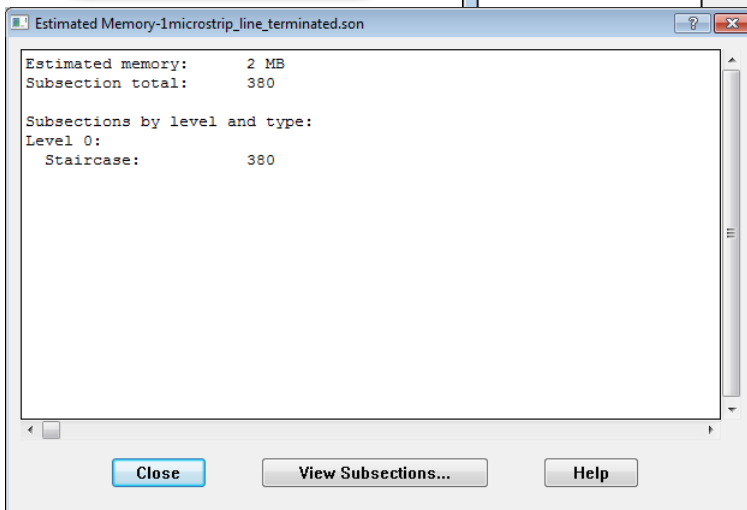
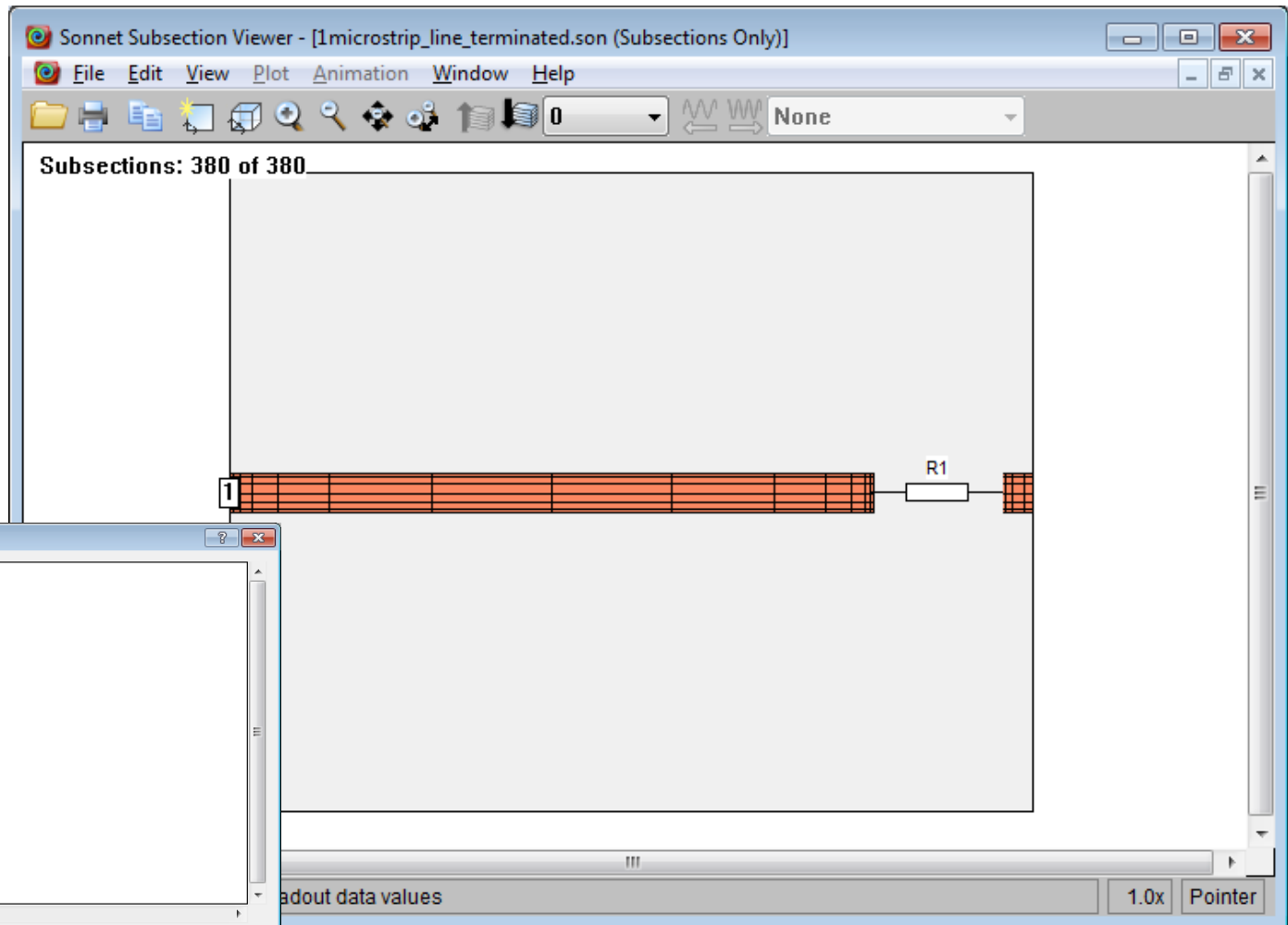
# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

So in about 12 straightforward steps, we have a model fully setup, ready to analyze.

Before we start the analysis, it is a good idea to subsection the model (Analysis -> Estimate Memory).

Taking this step will give us an estimate of the model size and will perform a number of checks. We can also view the subsectioning pattern.



# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

Use the menu command **Project -> Analyze** to launch the Analysis Monitor and run the analysis. Information is displayed while the analysis is running and clear indication of when it is finished.

We can plot the data during the analysis or when it is finished. Just click the **Response Viewer** button in the Tool Bar.

The screenshot shows the Sonnet Analysis Monitor window for the project '1microstrip\_line\_terminated.son'. The window title is 'Sonnet Analysis Monitor: 1microstrip\_line\_terminated.son 2.59 GHz Finished on PYTHON2 (Local)'. The menu bar includes File, Edit, View, Run, Project, and Help. The toolbar contains various icons, with the 'Analyze' icon (a green square with a white 'A') highlighted by a red box.

The main display area is divided into several sections:

- Memory:** 2 MB, Subs: 380, CM Cells: N/A, Threads: 1/4.
- Project:** 1microstrip\_line\_terminated.son, Frequencies: 6 Discrete [291 Adaptive], Time/Freq: 1 sec.
- Status:** 100% : Analysis Finished (displayed in a blue bar).
- Analysis completed:** Thu Jul 17 12:27:28 2014.
- Response Data:** A table showing the project status.
- Errors/Warnings:** A section for displaying errors or warnings.
- Timing Info:** A section for displaying timing information.
- Batch List:** A section for displaying a batch list.

The **Response Data** table is as follows:

| Project  | Status   |
|--|----------|
| Project: 1microstrip_line_terminated.son<br>0.1 to 3.0 GHz ABS | Finished |

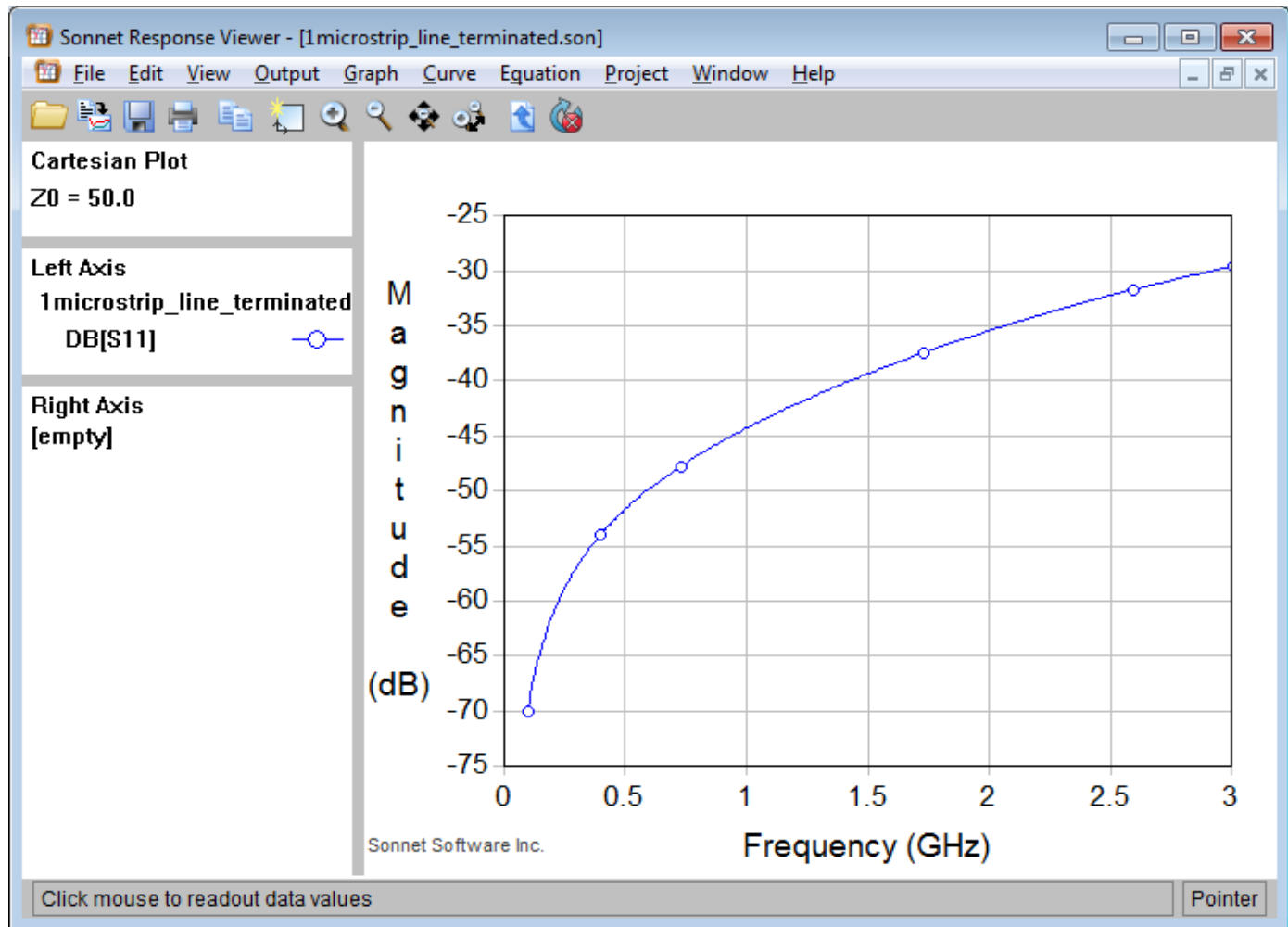
On the right side of the window, there are several buttons for managing projects:

- Add Project(s)...
- Remove Project
- Move to Next
- Move Up
- Move Down
- Move to Last

# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

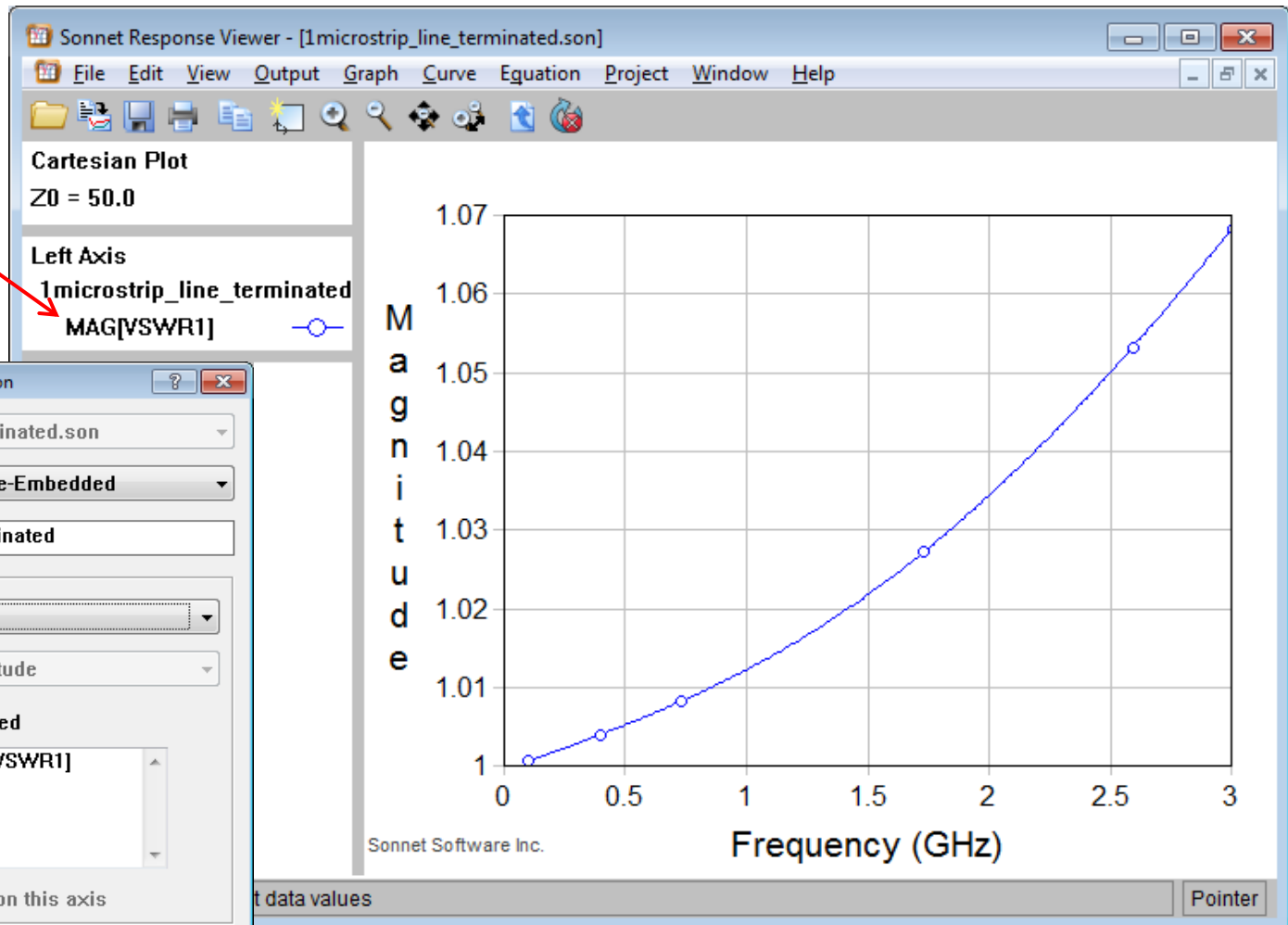
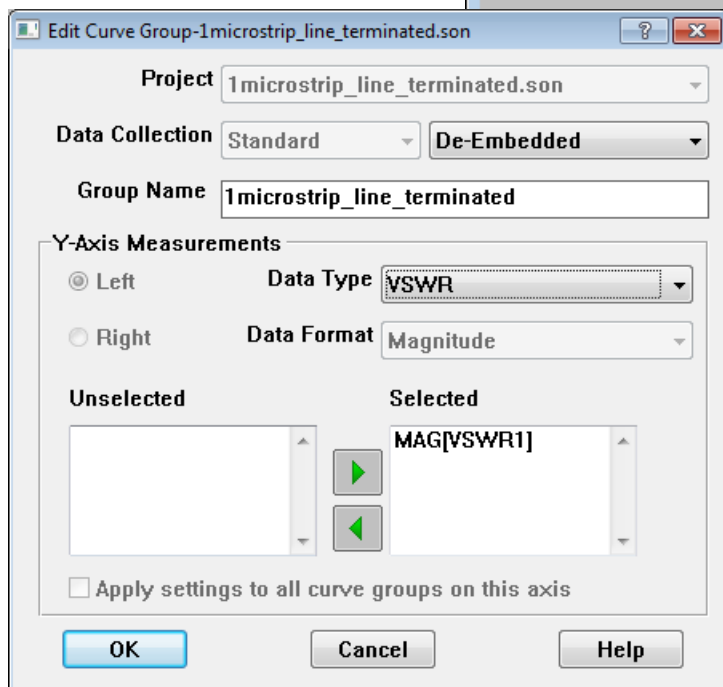
By default, a Cartesian graph of S11 in dB, will be plotted in the Response Viewer.



# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

We can change the displayed Data Type by right clicking on quantity in the left legend region and selecting the command Edit Curve Group. Shown here is the VSWR

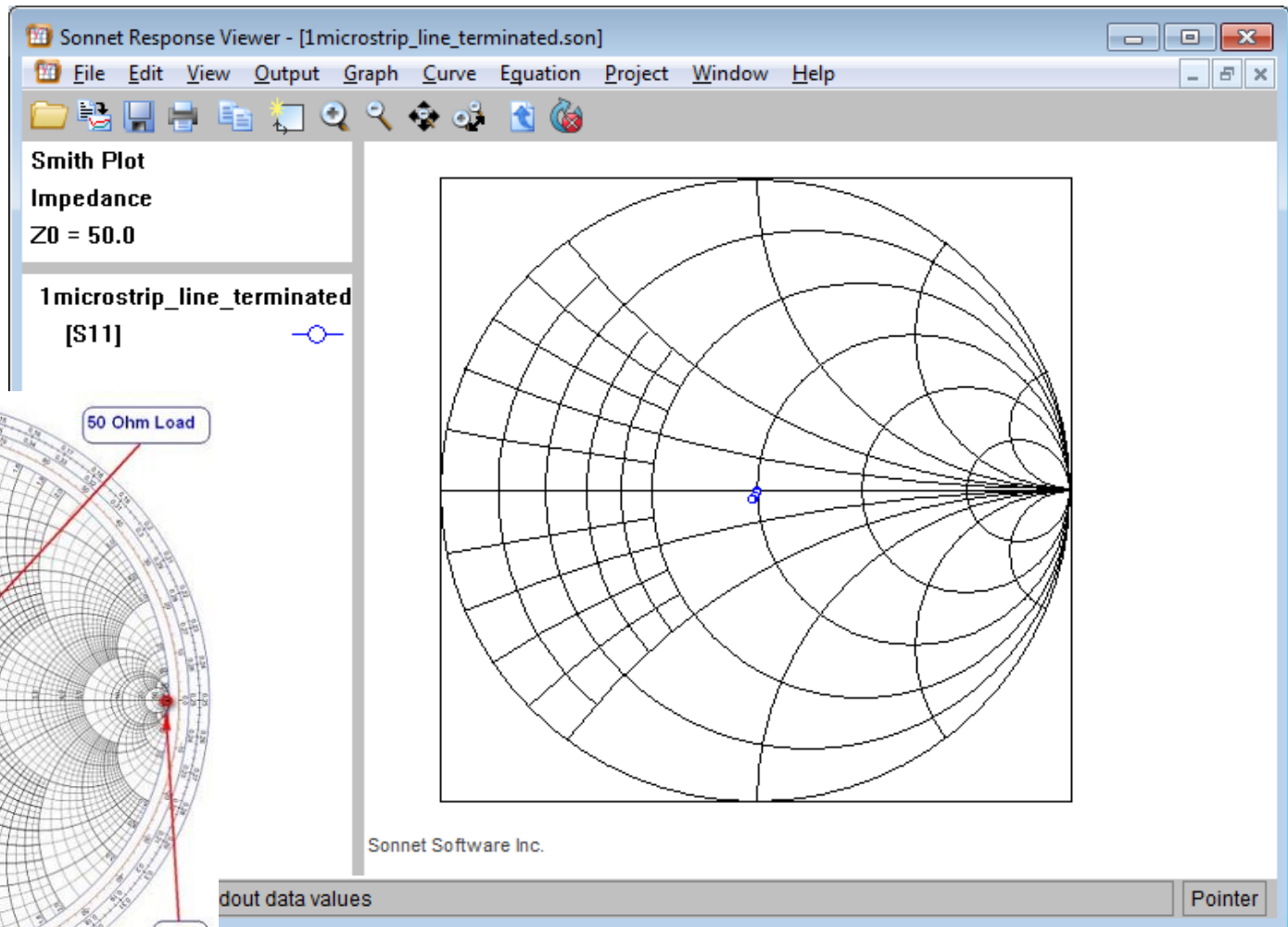
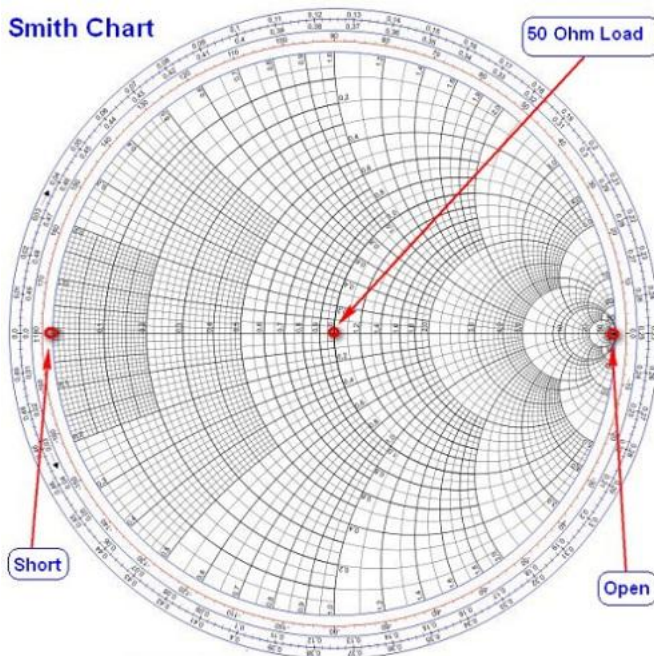


# Advanced Digital Design using Sonnet

## SONNET Tutorial – Terminated Microstrip Line

We can change the graph to a Smith Chart using the menu command Graph -> Type -> Smith. Below is a quick explanation of how to interpret impedances on a Smith Chart.

Smith Chart



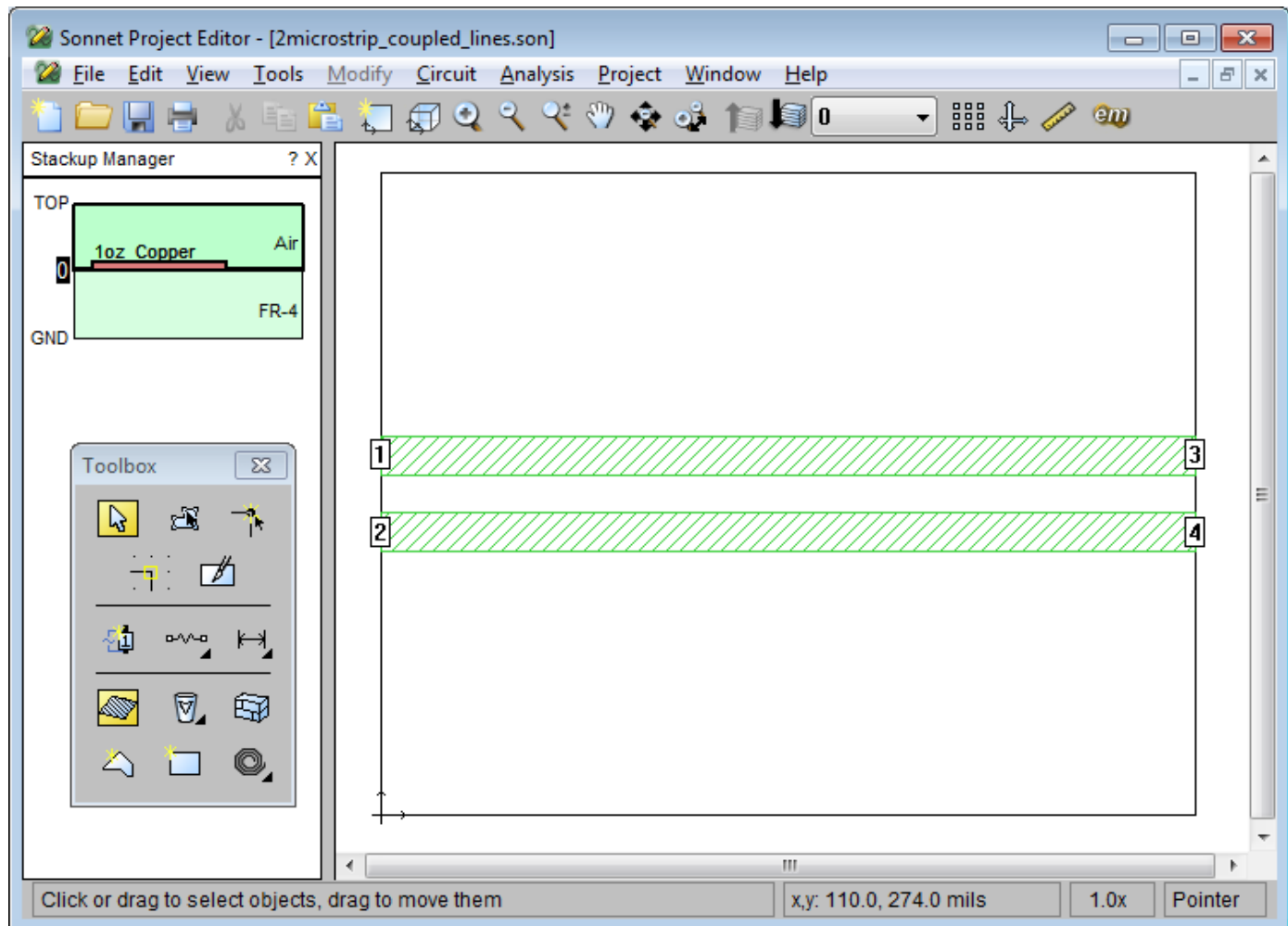
# Advanced Digital Design using Sonnet

## SONNET Tutorial – Coupled Microstrip Lines

We can save the previous model under a new name and quickly modify it to create a 4-port coupled line model.

Below is a summary of the steps:

- 1) Delete the resistor and small polygon.
- 2) Use the menu command Tools -> Reshape to stretch the trace polygon to the right wall.
- 3) Use copy/paste or Modify -> Move to create a second trace.
- 4) Use Modify -> Center -> Vertically to position the traces.
- 5) Add or edit the ports as required.

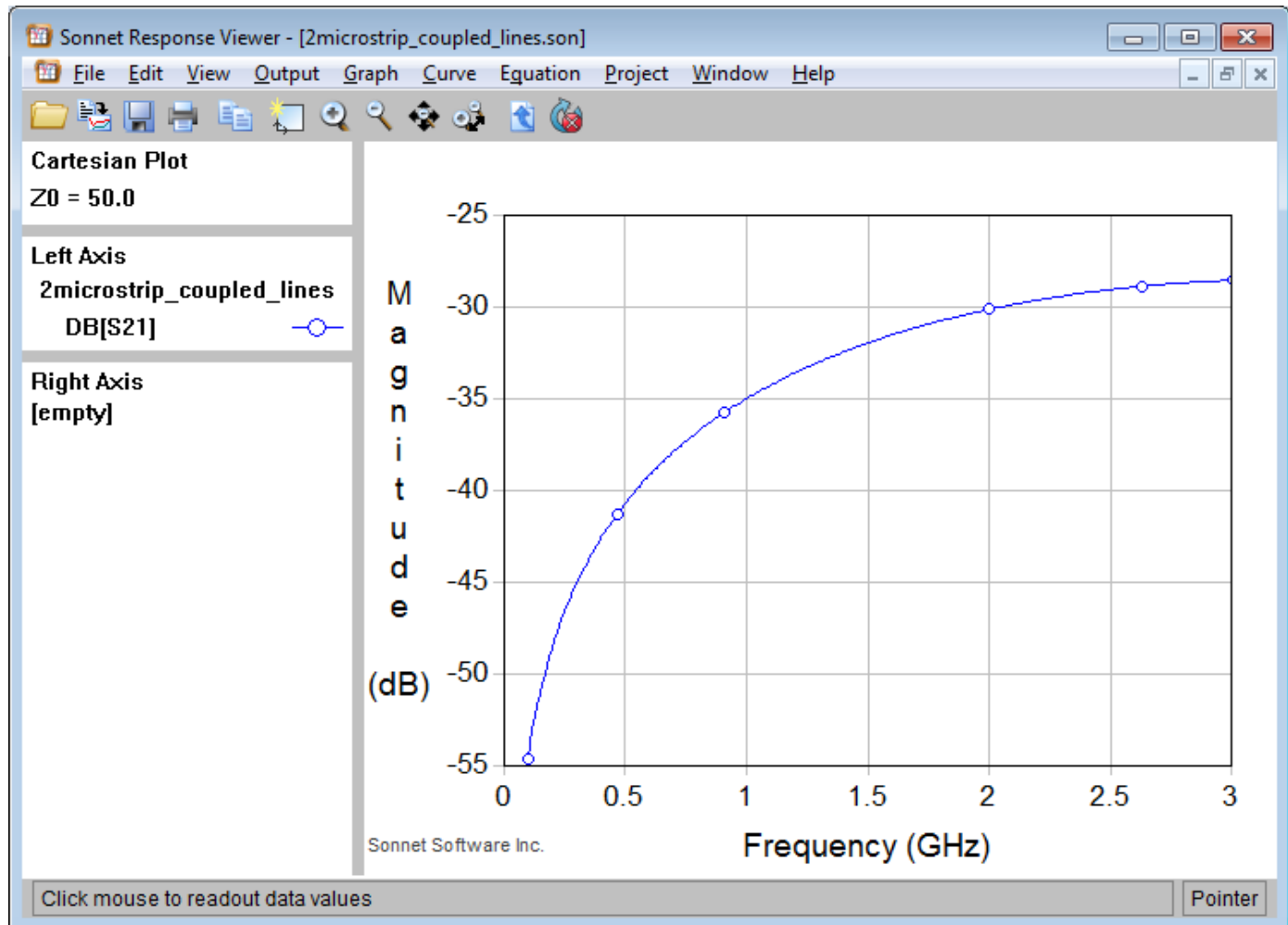




# Advanced Digital Design using Sonnet

## SONNET Tutorial –Coupled Microstrip Line

With this model we might be interested in the crosstalk between the traces. We can plot the Near End Crosstalk (NEXT) using the dB[S21] S-parameter.



# Advanced Digital Design using Sonnet

## SONNET Tutorial – Coupled Microstrip Line

From the Response Viewer, we can extract a number of output files that can be useful for time domain analysis:

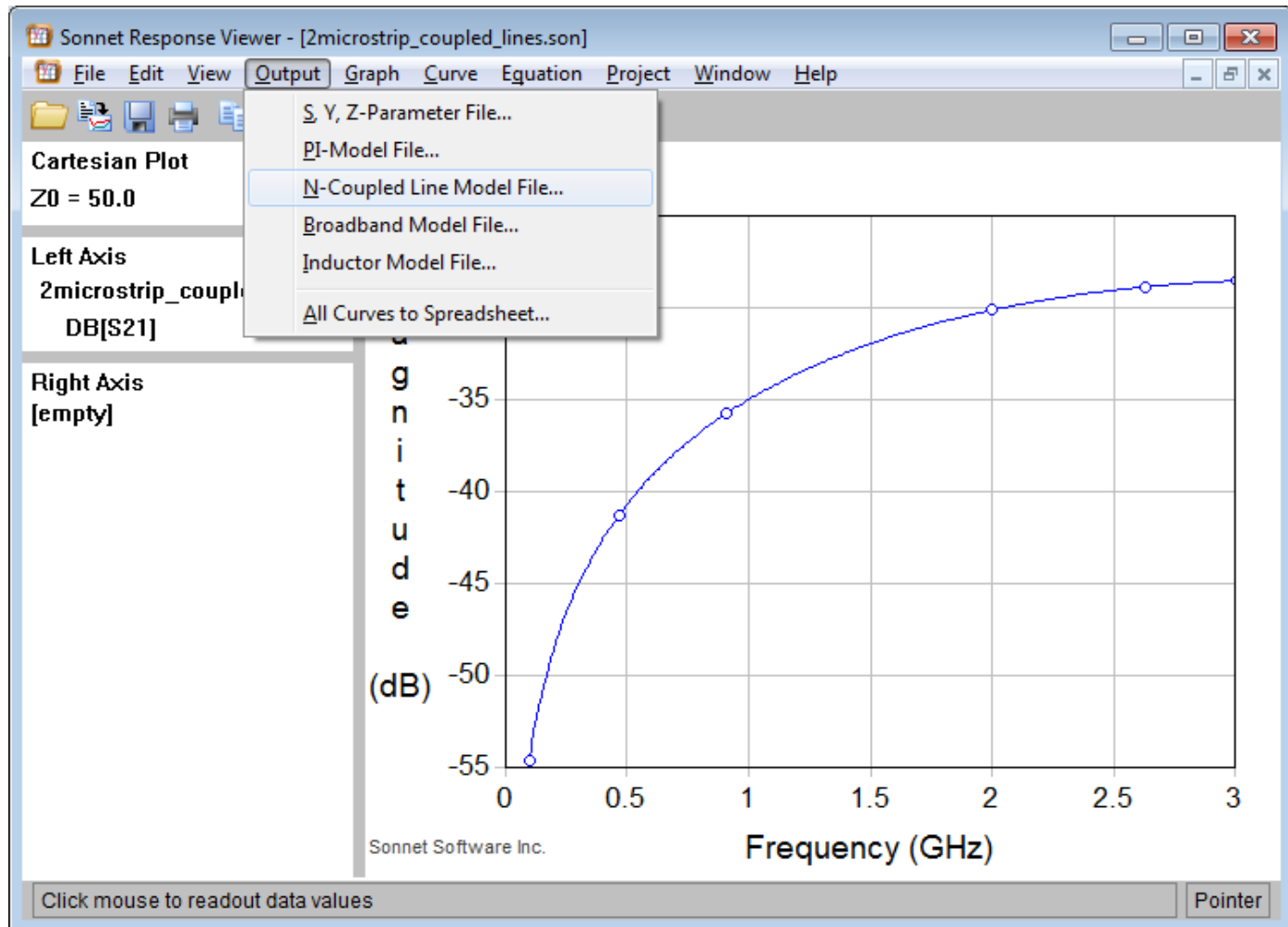
**S, Y, Z-parameter file** – some time domain tools can work directly with S-parameter files. Historically, this approach has not been efficient.

**Pi-Model file** – This file contains a number of narrowband Pi model equivalent circuits. Typically, the circuit is somewhat human meaningful for simple models.

**N-Coupled Line file** – This extraction is useful in creating RLGC matrices for transmission line models. This file can then be associated with a Transmission Line element in SPICE or similar tool.

**Broadband Model file** - This file contains a single equivalent circuit for the whole frequency sweep. It contains sources and the circuit is not human meaningful.

**Inductor Model file** – There are two fixed topologies available for inductor fitting. These are physically meaningful equivalent circuits and can be inserted as schematics in time domain tools.

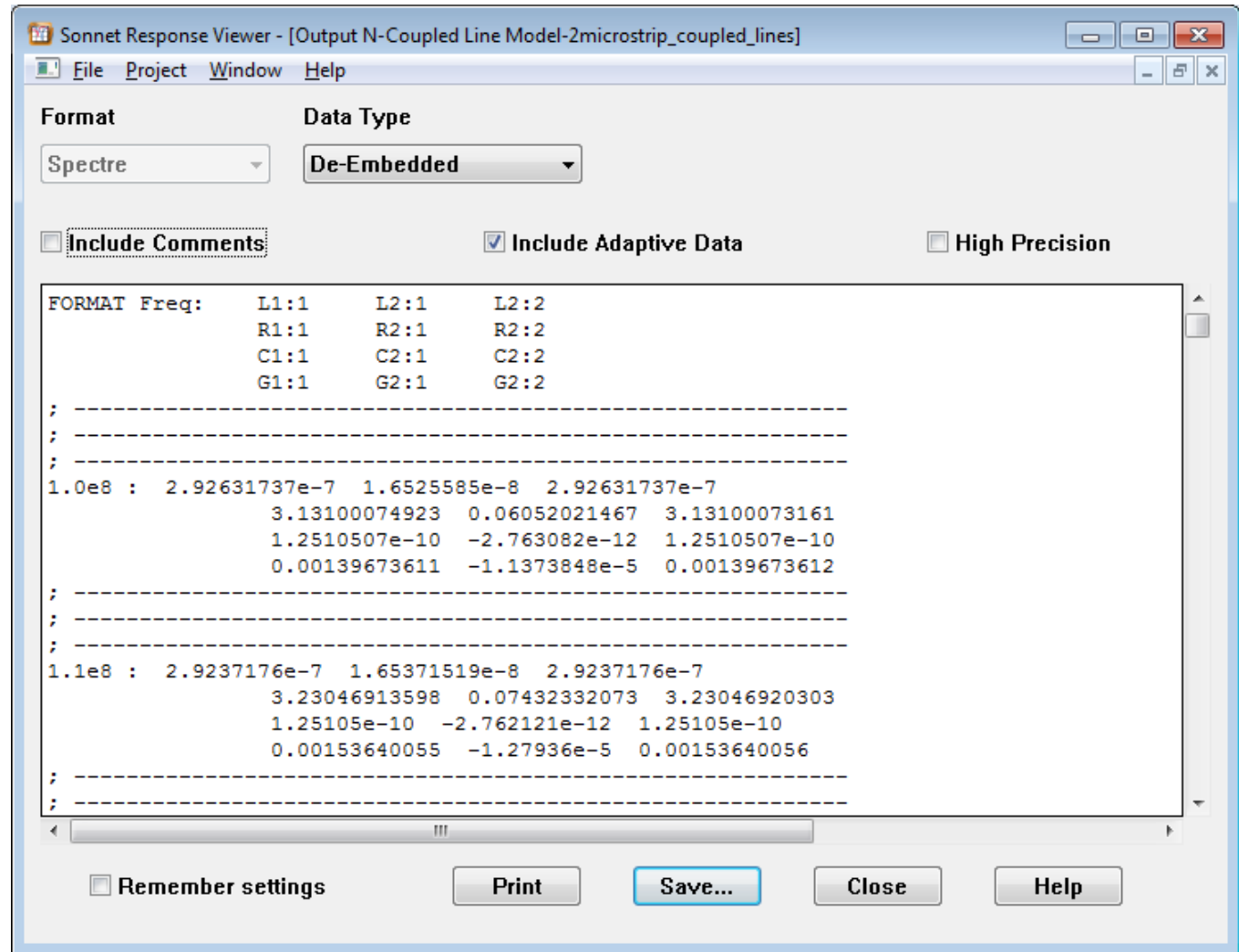


# Advanced Digital Design using Sonnet

## SONNET Tutorial – Coupled Microstrip Line

With a coupled line model, the N-Coupled Line output file is likely the most useful.

We can see the format and the RLGC matrices for the coupled transmission lines.



Sonnet Response Viewer - [Output N-Coupled Line Model-2microstrip\_coupled\_lines]

File Project Window Help

Format: Spectre Data Type: De-Embedded

☐ Include Comments ☒ Include Adaptive Data ☐ High Precision

```
FORMAT Freq:  L1:1    L2:1    L2:2
              R1:1    R2:1    R2:2
              C1:1    C2:1    C2:2
              G1:1    G2:1    G2:2

; -----
; -----
; -----
1.0e8 :  2.92631737e-7  1.6525585e-8  2.92631737e-7
              3.13100074923  0.06052021467  3.13100073161
              1.2510507e-10 -2.763082e-12  1.2510507e-10
              0.00139673611 -1.1373848e-5  0.00139673612

; -----
; -----
; -----
1.1e8 :  2.9237176e-7  1.65371519e-8  2.9237176e-7
              3.23046913598  0.07432332073  3.23046920303
              1.25105e-10 -2.762121e-12  1.25105e-10
              0.00153640055 -1.27936e-5  0.00153640056

; -----
; -----
; -----
```

☐ Remember settings Print Save... Close Help

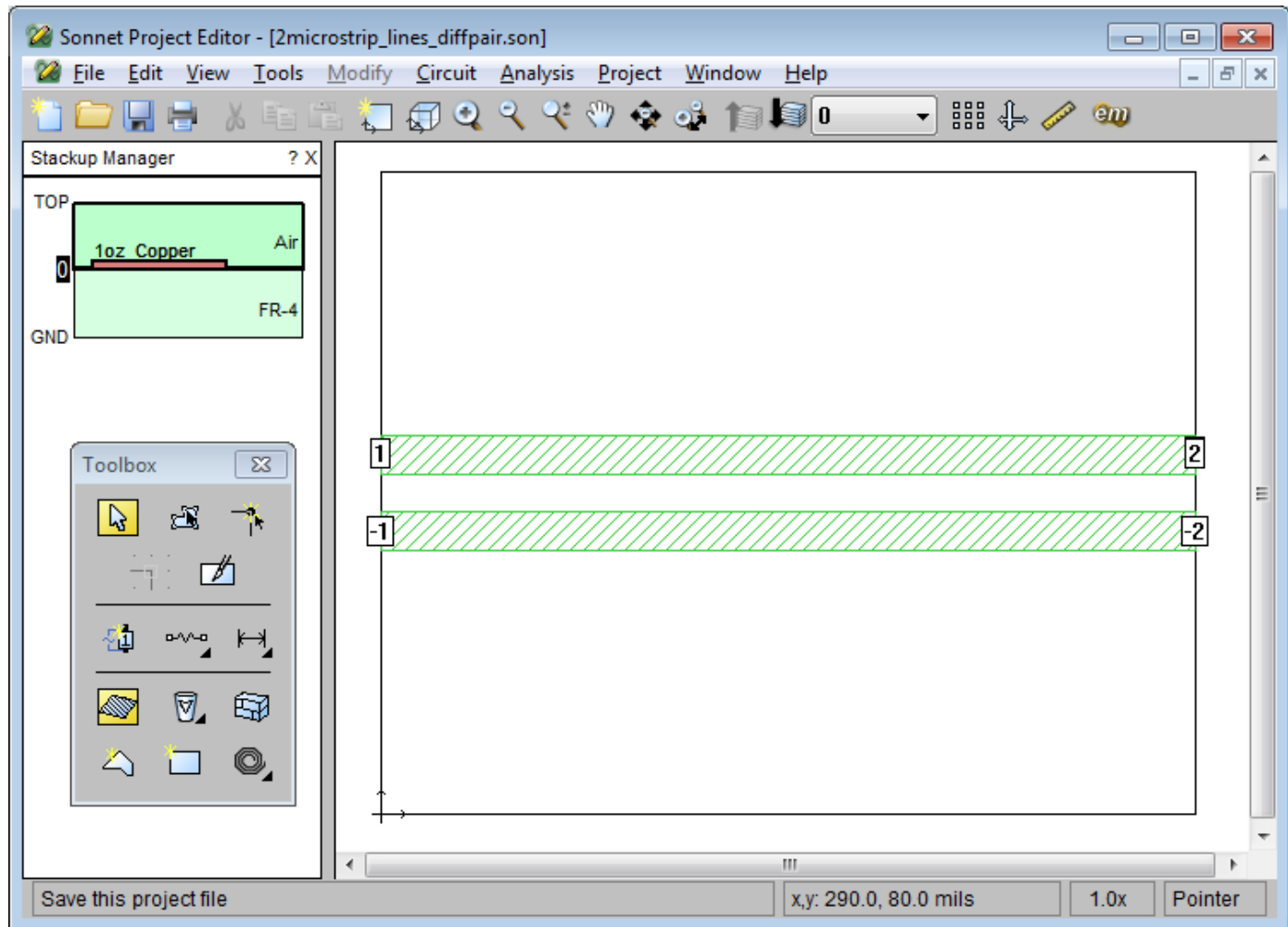
# Advanced Digital Design using Sonnet

## SONNET Tutorial – Differential Pair Microstrip Lines

Many digital circuits use differential signal lines instead of single ended lines. We can work with differential pairs in Sonnet, simply by editing the port numbers and creating +/- port pairs.

Here we saved the previous model under a new name and configured it as a differential pair.

For some added data, the “Compute Current Density” box was checked under the Analysis Setup dialog box

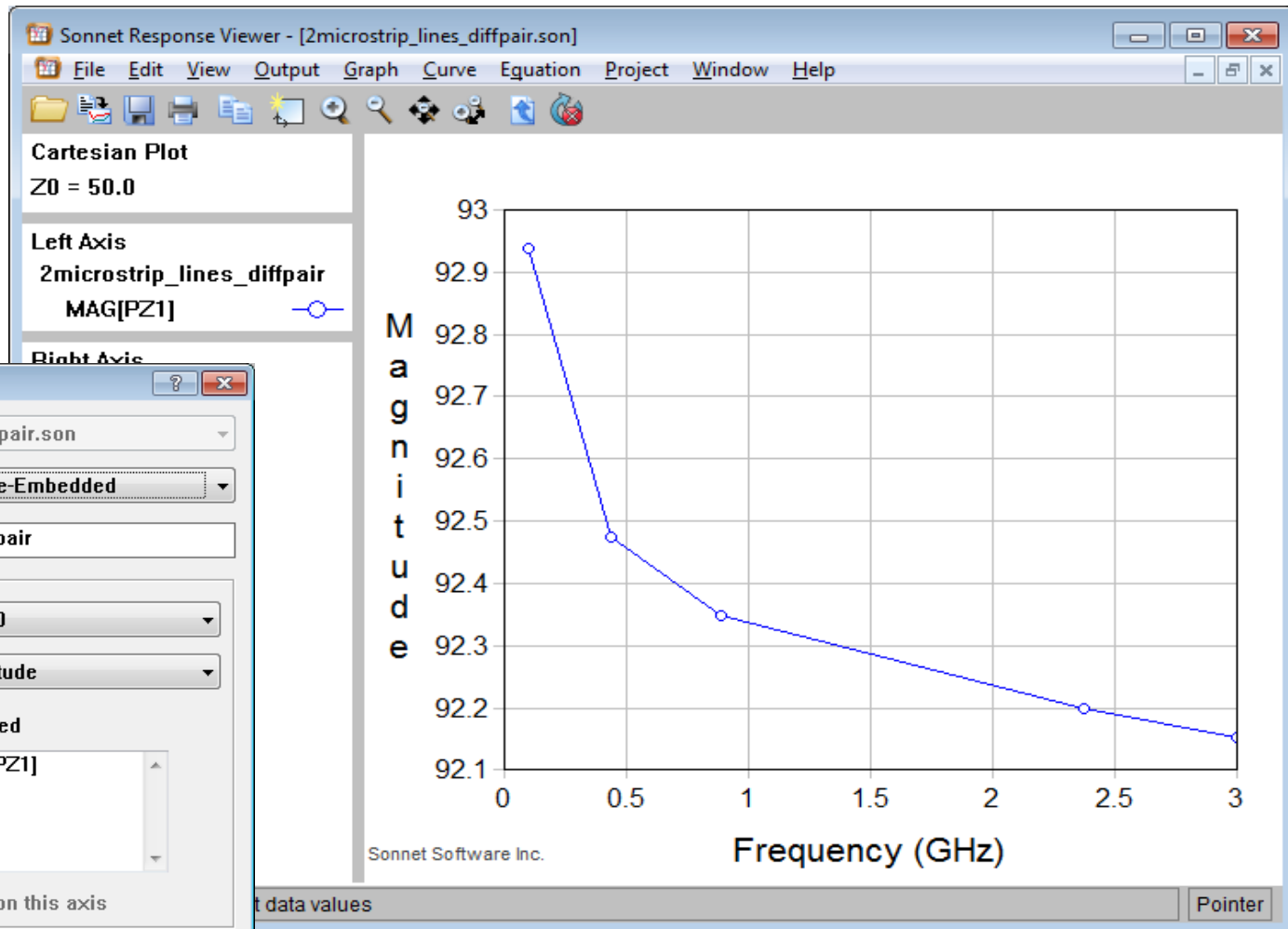
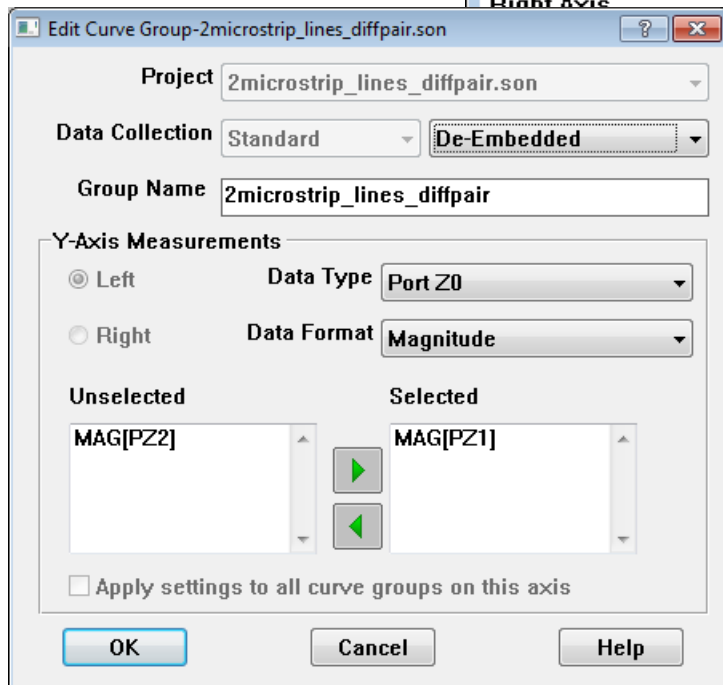


# Advanced Digital Design using Sonnet

## SONNET Tutorial – Differential Pair Microstrip Lines

Along with the S-parameters mentioned previously, we can plot the Port Z<sub>0</sub> of the differential pair. To do so, use the Edit Curve Group command and change the Data Type.

Note that data points are only available at frequencies where a full analysis was performed.

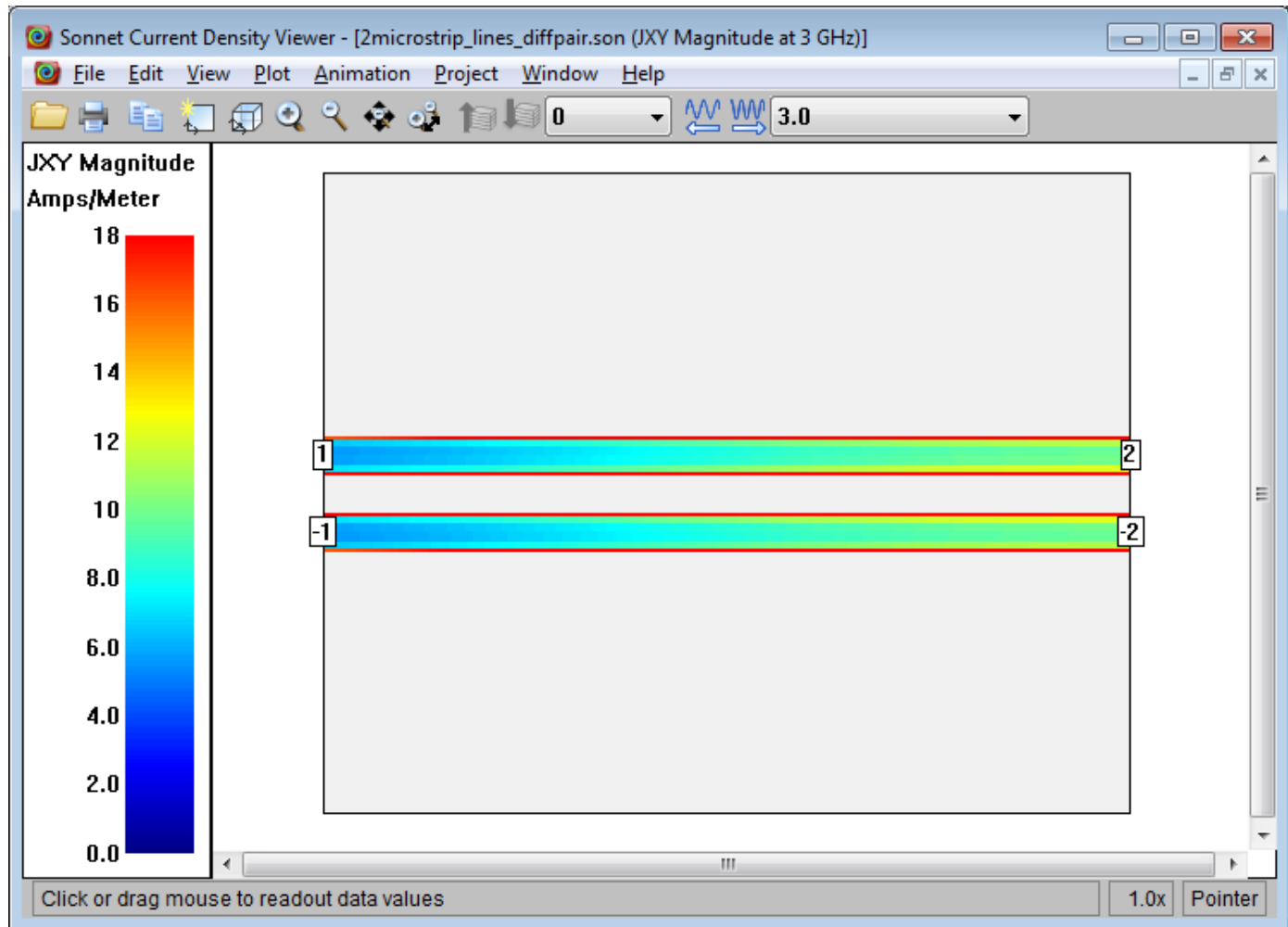


# Advanced Digital Design using Sonnet

## SONNET Tutorial – Differential Pair Microstrip Lines

Along with the frequency domain data, the Sonnet solver can also compute the current density. You can plot this data using the menu command Project -> View Current in the Project Editor window.

Shown here is the current density for the differential pair at 3 GHz. There is high current density on the trace edges, which is normal for high frequency circuits. There is also generally lower current density on the left side of the traces than on the right side. This is caused by the mismatch between the differential pair  $Z_0$  value (92.1 Ohms) and the port terminations (50 Ohms). This is the standing wave effect.



# Electromagnetic Modeling of Transmission Lines using Sonnet

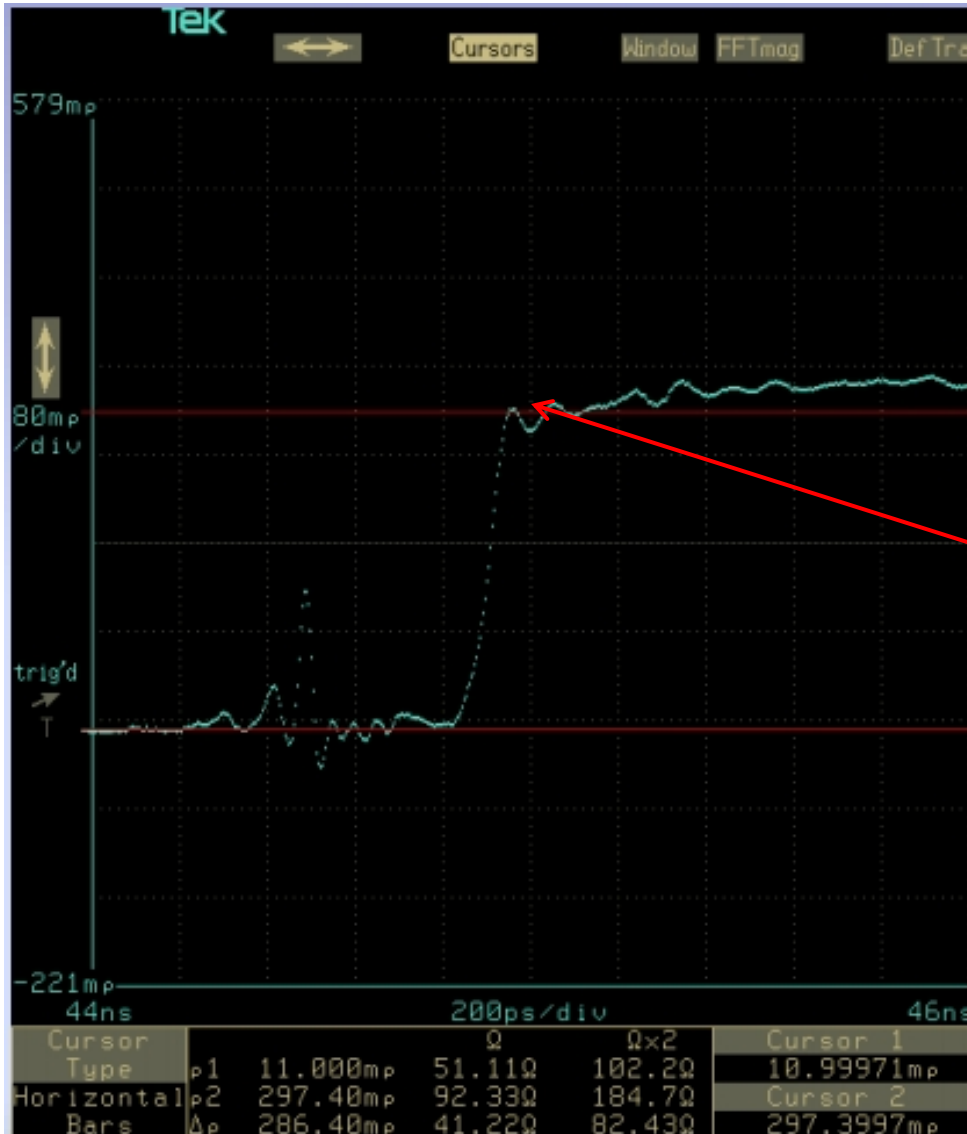
## Conclusions of Sonnet as a Digital Signals Integrity Simulation Tool

**There are a number of SI applications that can be modeled and Simulated in Sonnet. Some useful ones are:**

1. Compute  $Z_0$  for unusual stackups and geometries - Many multilayer PCB designs use multiple materials with different  $\epsilon_r$  values. It might also contain some asymmetry in the trace placement in the stackup. Sonnet allows the user to compute a  $Z_0$  value.
2. Study various transmission line circuits with both single ended and differential excitation/termination.
3. Study the effect of multilayer vias in the signal path
4. Study crosstalk between transmission lines.
5. Study the influence of anisotropic laminate materials and metal roughness of copper foils on the signal path.
6. You can use Sonnet as a standalone tool where you create the geometry and layer stackup directly within the Sonnet Project Editor interface. You can also work within the Microwave Office framework and translate an existing layout into Sonnet. Both methods are quite useful. Sonnet also has nice interfaces into Agilent ADS and Cadence Virtuoso. Sonnet also reads and writes GDSII and DXF files
7. Sonnet does contain its own Response Viewer in which you can plot S, Y, Z-parameters,  $Z_{in}$ , and other frequency domain quantities. Sonnet also computes  $Z_0$  and  $\epsilon_r$  effective at full analysis frequencies and these quantities can also be plotted.
8. Another feature is the equation capability in the Response Viewer. There are built-in equations or the user can define his/her own. An example of the built-in equations is Group Delay.
9. Sonnet can compute the current density within a circuit and Ground paths illustrated

# Digital Design Validation Tools

## SI Verification Tool –Time Domain Reflectometry (TDR) <sup>1</sup>



Time Domain Reflectometry measures the reflected response of a circuit to an applied pulse, for a defined system impedance

TDR patterns are typically used to detect a short or open circuit, test proper termination impedance, and characterize interconnect discontinuities.

In evaluating the TDR as a digital signal diagnostic instrument, the source is a fast, typically  $\leq 40$ ps, Voltage step generator. The frequency content of the step depends on the rise time of the pulse.

This TDR measurement illustrates the reflected signal looking from a 50 Ohm pulse source into a 100 Ohm termination. There is a pronounced step at the location of the mismatched termination, because it deviates from the 50 Ohm system impedance.

<sup>1</sup> Hall, Hall, and McCall, *High-Speed Digital System Design*, John Wiley & Sons Inc., 2000: 284 - 303

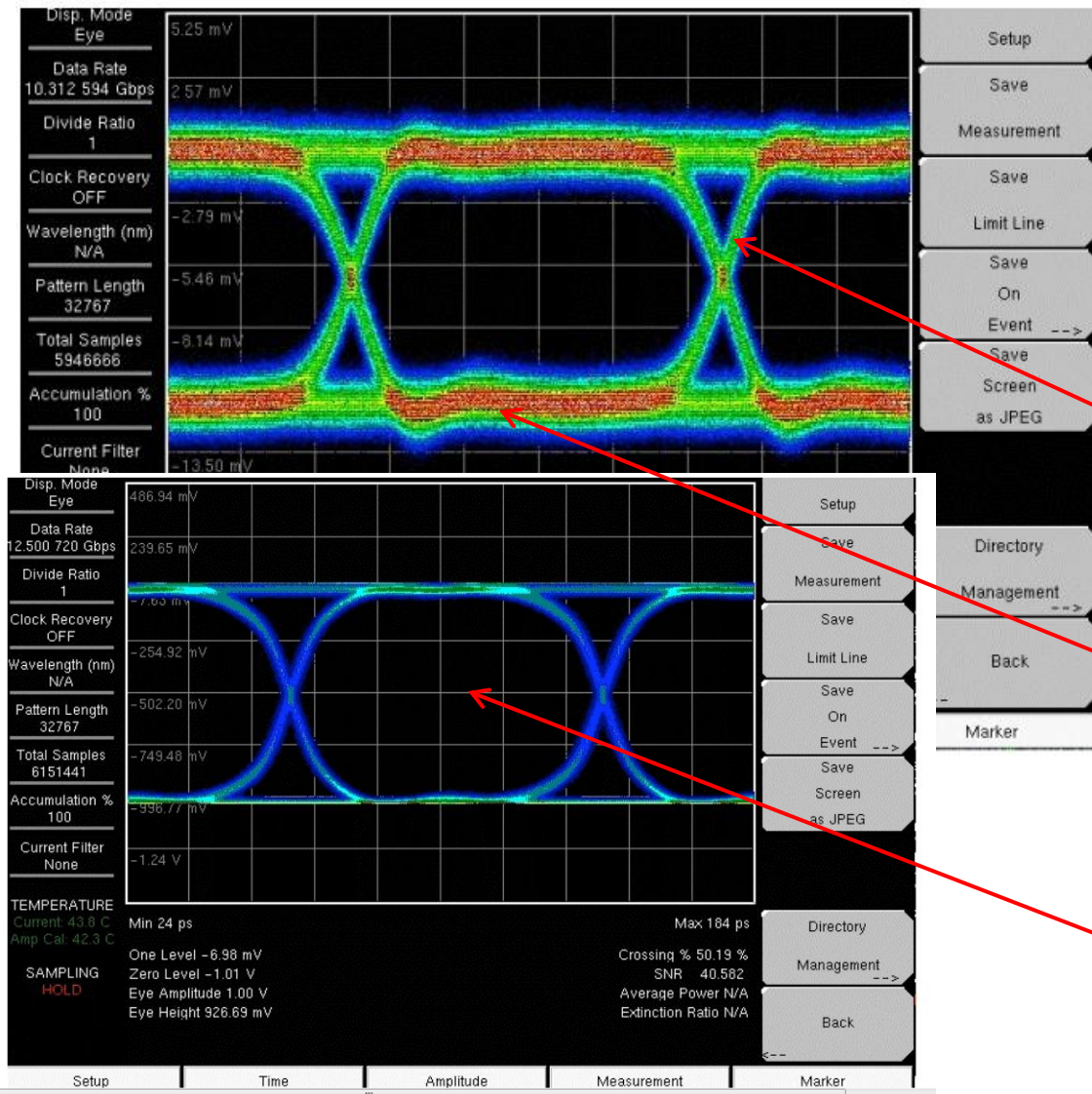
$$\rho = \frac{V_{reflected}}{V_{incident}} = \frac{Z_{load} - Z_0}{Z_{load} + Z_0}$$

$$Z_{DUT} = Z_0 \cdot \frac{1 + \rho}{1 - \rho}$$



# Digital Design Validation Tools

## SI Verification Tool – Eye Diagram Mask



The Eye Diagram Mask is a measurement of the overall digital link in the time domain. Many bit sequences are overlaid creating a series of “eye” patterns. Much can be learned about the path characteristics from the Eye Diagram.

This test is typically used to verify long communications links (optical and wireless), but now is also used in new digital serial link standard compliance testing procedures

This Eye Diagram measurement exhibits JITTER that appears as a timing misalignment error on the rising and falling edges.

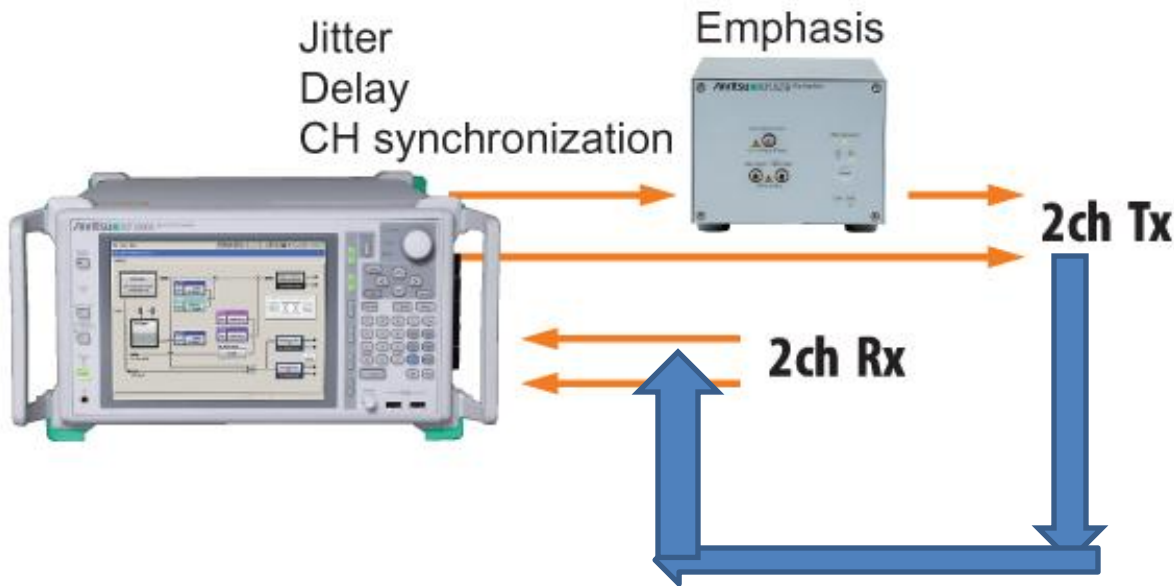
This Eye Diagram measurement also exhibits excess NOISE that appears as widening of the amplitude bands that the signal levels fall within.

NOISE and JITTER cause the Eye pattern to close and will eventually lead to data errors.

This Eye Diagram illustrates a serial link with lower NOISE and JITTER.

# Digital Design Validation Tools

## SI Verification Tool – Bit Error Rate Tester (BERT) <sup>3</sup>



Local/Remote Node in Data Loopback Node

BERT data generation is a common in-production serial digital data test instrument. This is useful in testing end-to-end communications link. Wireless carriers like Verizon and AT&T use BERT testing daily to test end-to-end connectivity and to insure the link is operational. For development purposes, Jitter, Delays, and Sync errors can be injected and the tolerance for these specific data errors measured.

Digital pseudorandom patterns are generated and sent (see 2ch Tx), the remote node is set to "loopback", and the patterns are matched to what was sent and any errors are indicated as " $n \times 10^{-6}$  errors."

<sup>3</sup> Johnson and Graham, *High Speed Signal Propagation*, Prentice Hall, 2003: 650

# Digital Design Validation Tools

## SI Verification Tool – Vector Network Analyzer (VNA)



The Vector Network Analyzer (VNA) measures the network parameters of a DUT in the frequency domain. Typically, reflected and transmitted signals are measured for a 2-port device. This information is usually displayed as S-parameters.

VNA S-parameter measurements are flexible and can yield a wealth of information about the DUT over wide or narrow frequency band.

This VNA measurement is of S11 with dB units. It is the measurement of the reflected signal at Port 1. More negative dB values indicate smaller reflected signal levels and therefore a better match between the DUT input impedance and the port termination value (typically 50 Ohms).

$$Z_{input(DUT)} = Z_0 \cdot \frac{1 + S_{11}}{1 - S_{11}} \quad S_{11} = \frac{V_{reflected1}}{V_{incident1}} = \frac{Z_{input(DUT)} - Z_0}{Z_{input(DUT)} + Z_0}$$

# Tutorial Conclusions

- There are many Signal Integrity challenges in today's high speed digital designs.
- Digital design engineers need to take advantage of both the many software and hardware tools available to help understand Signal Integrity problems before releasing a design for manufacture.
- SONNET provides Digital SI simulation capabilities to model 3D planar circuits in the frequency domain
- Digital System tools Testing Methodology, such as TDR, VNR, BERT, Eye Diagram, are useful for In-practice Signals Integrity Verification & Diagnostics